MS-7592

Version 10

CPU:

Intel Conroe (95W Dual core)

System Chipset:

Intel G41 - MCH (North Bridge)
Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI
HD -- ALC888S
LPC Super I/O -- F718829G
LAN-- REALTEK RTL8111D Co-lay RTL8103E
CLOCK -- RTM875-605

Main Memory:

DDR II *2 (Max 4GB)

Expansion Slots:

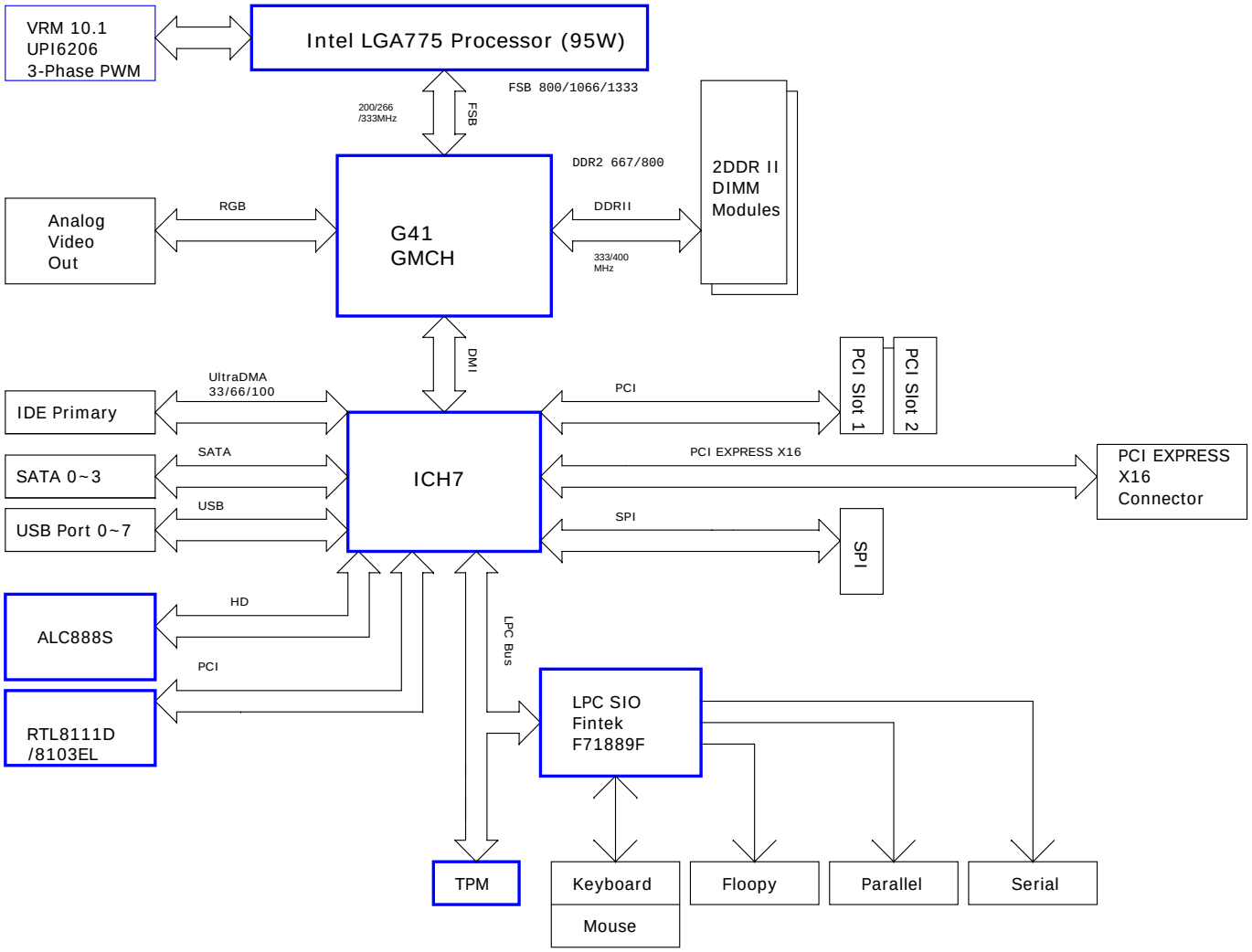
PCI2.3 SLOT * 2

PCI EXPRESS X16 SLOT

ST PWM:

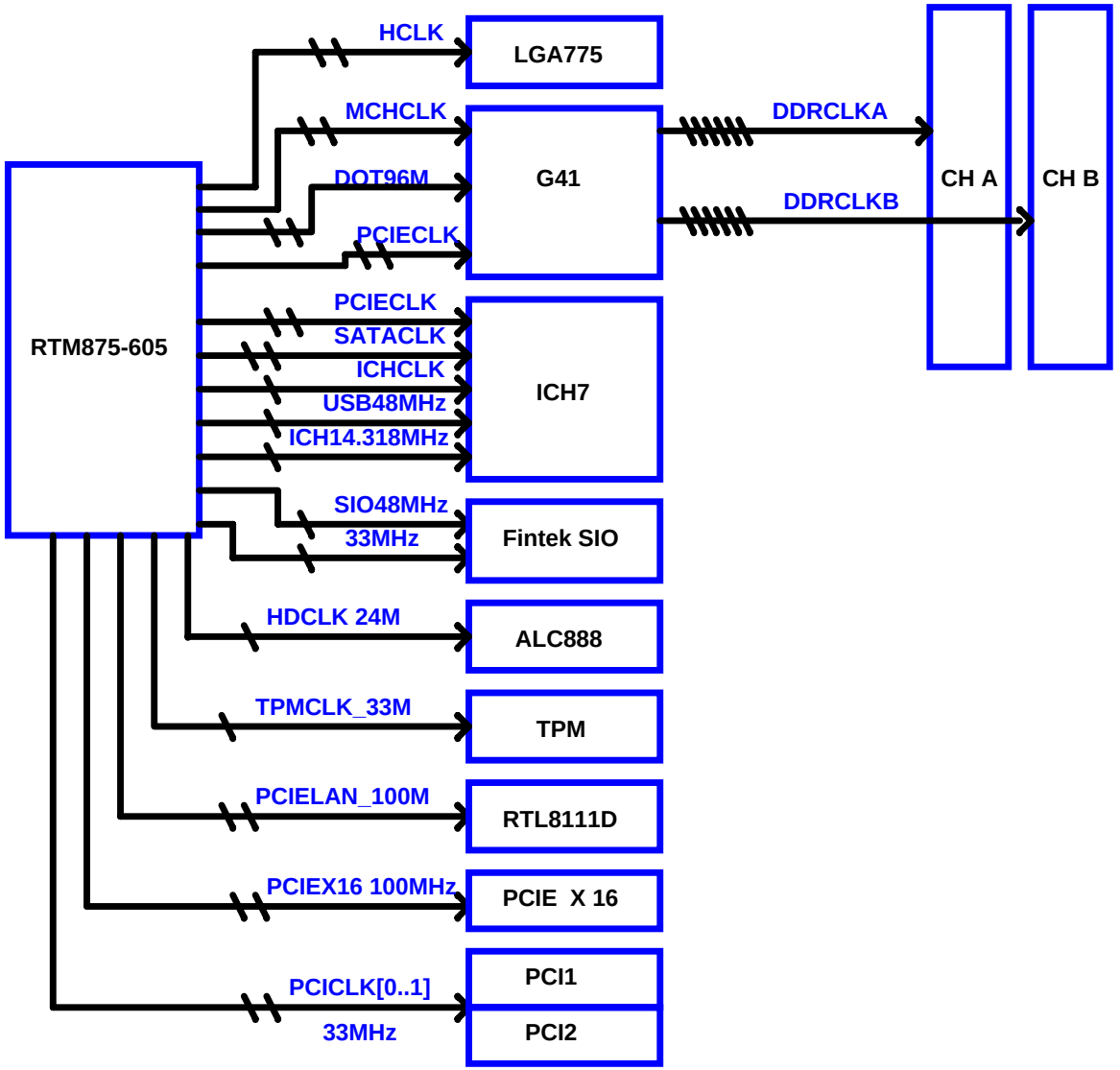
Controller: 3 PHASES

Block Diagram

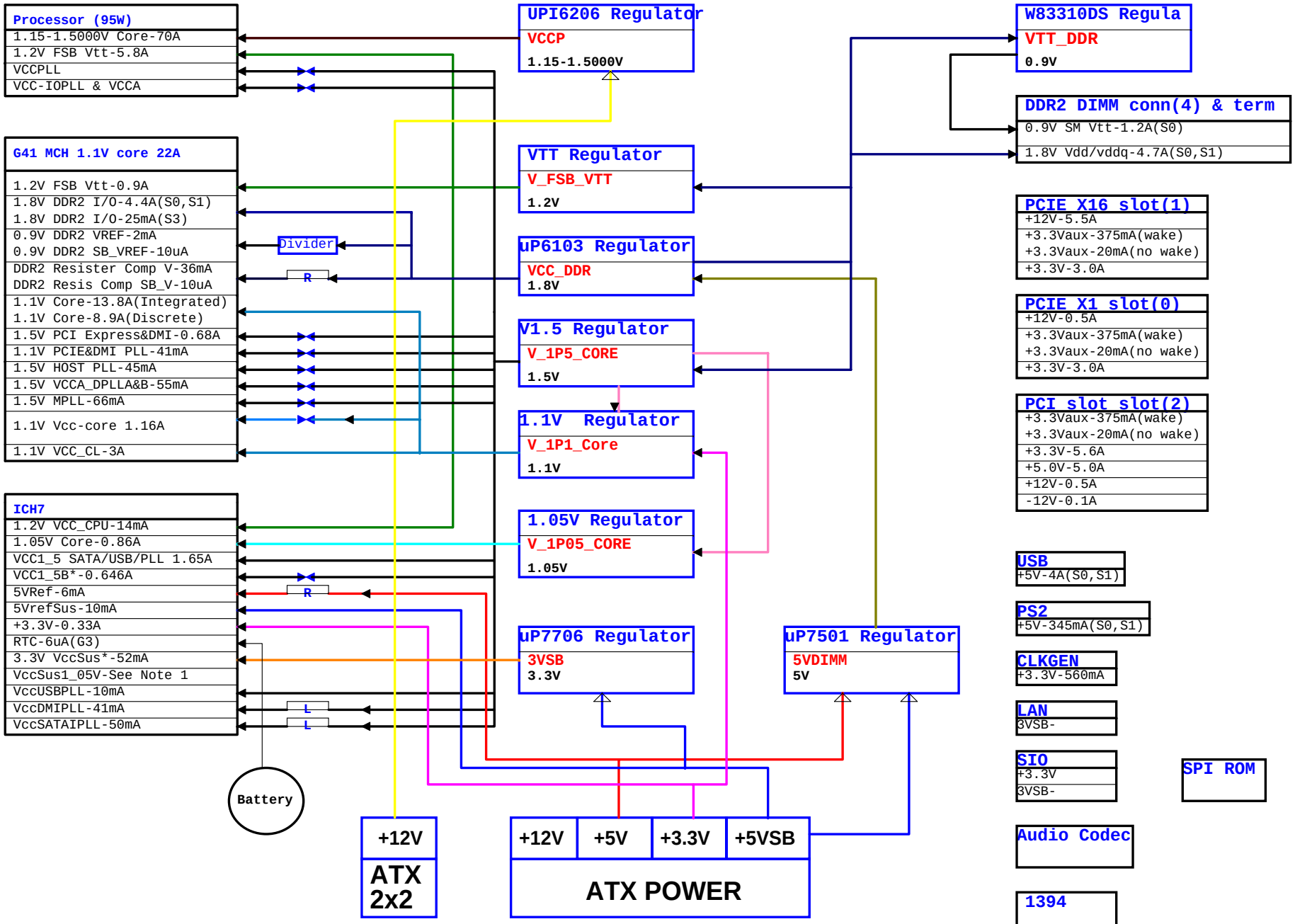


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7592	
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 1.1
Date: Monday, December 15, 2008	Sheet 2 of 33	

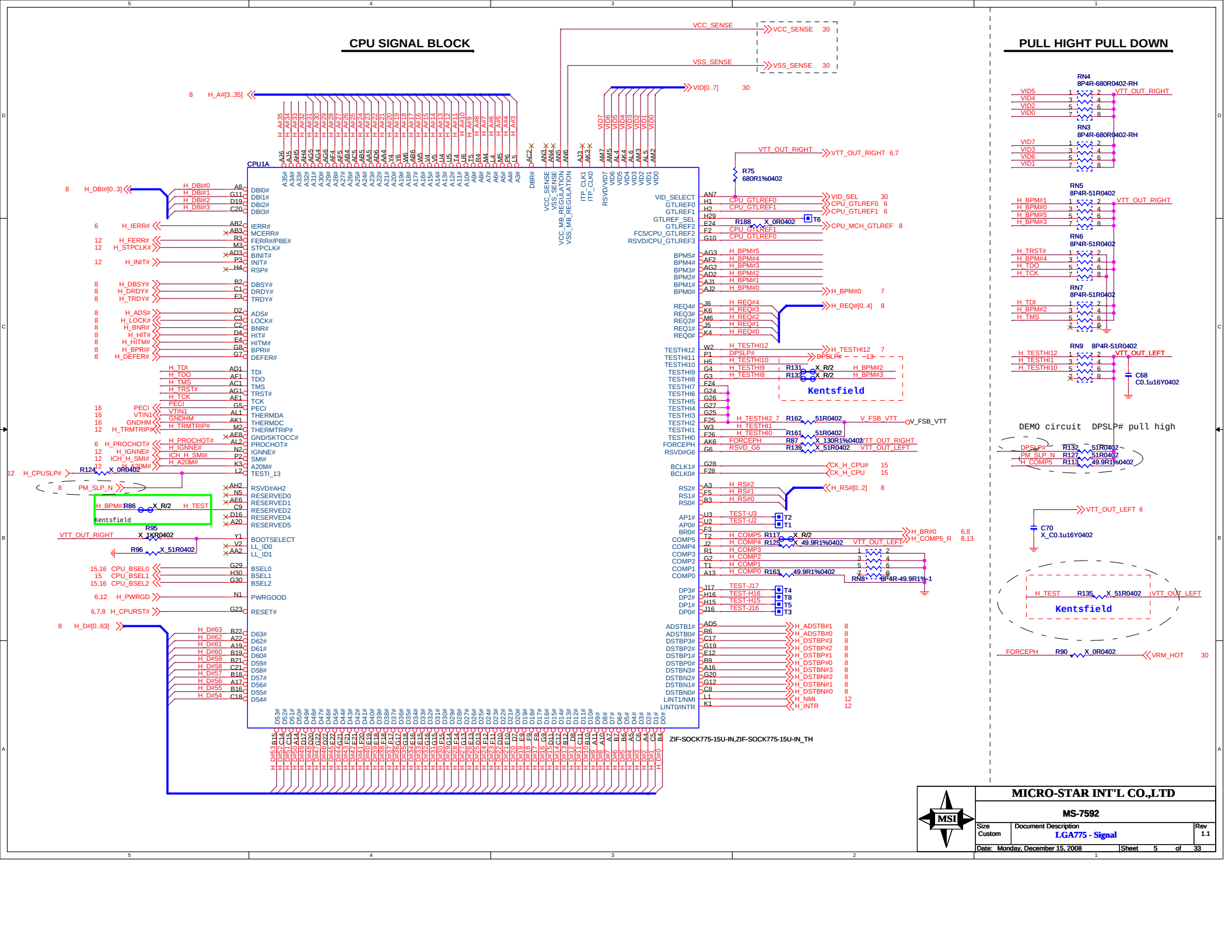
CLOCK MAP

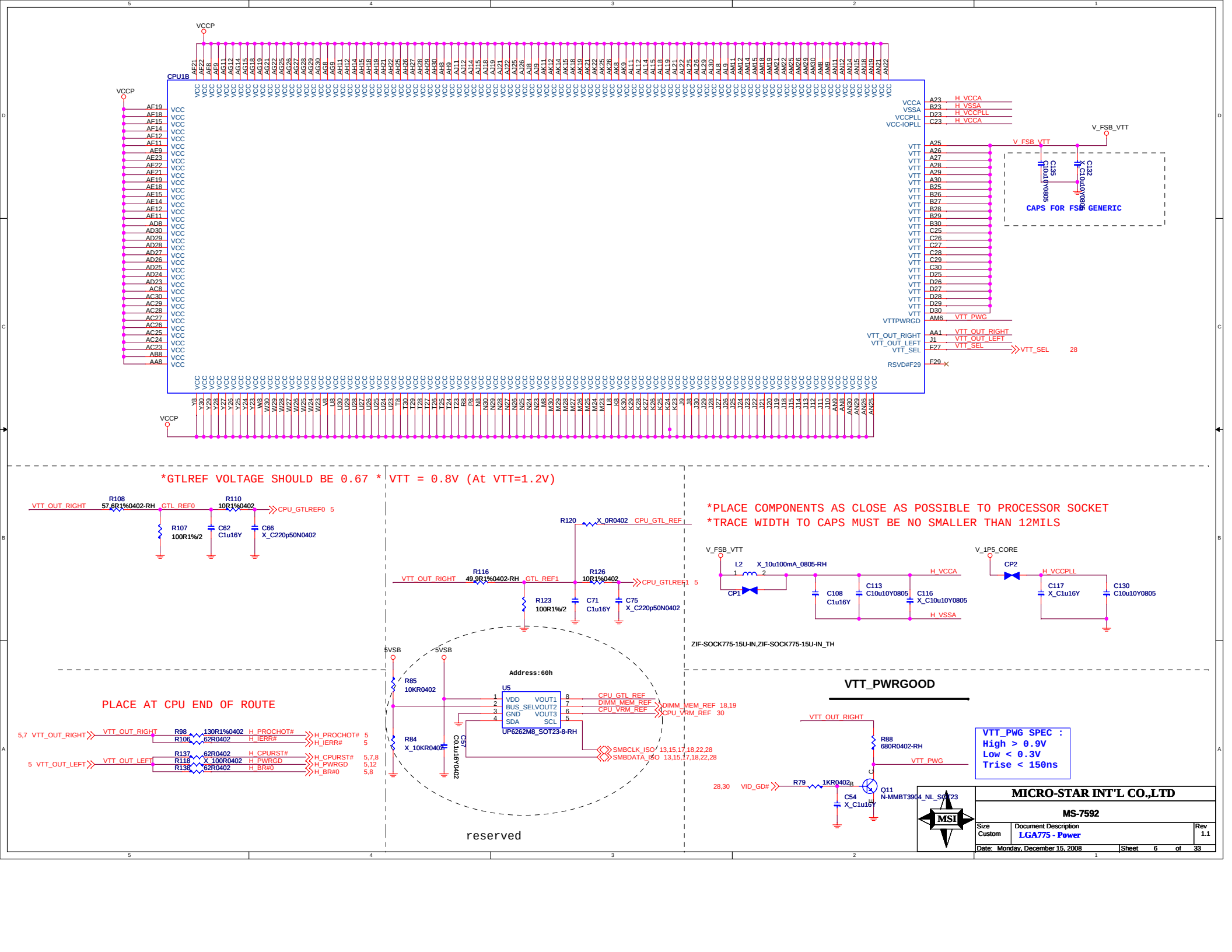


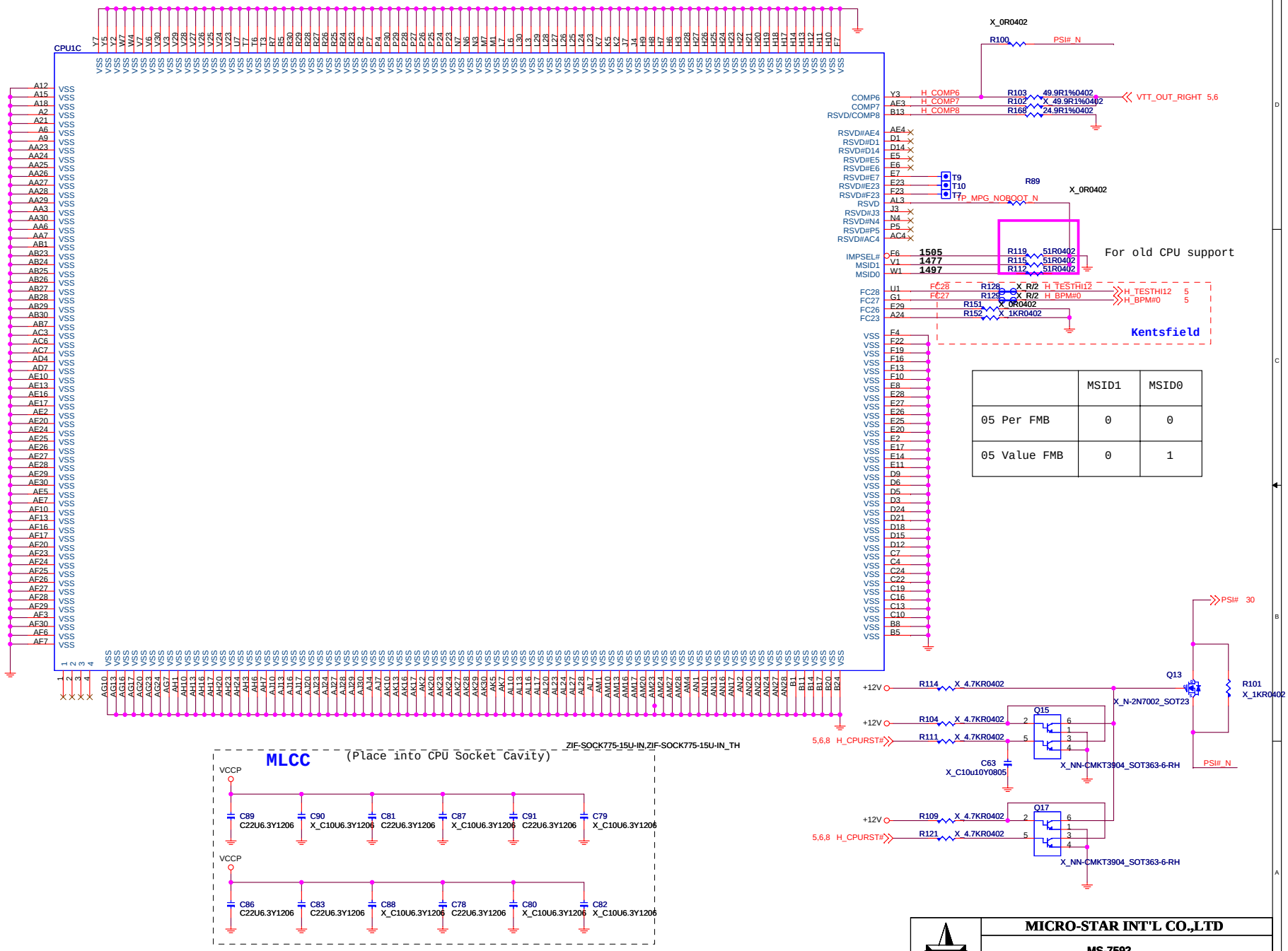
MICRO-STAR INT'L CO.,LTD		
MS-7592		
Size: Custom	Document Description: CLOCK MAP	Rev: 1.1
Date: Monday, December 15, 2008	Sheet 3 of 33	



MICRO-STAR INT'L CO.,LTD	
MS-7592	
Size: Custom	Document Description: LGA775 - Signal
Rev: 1.1	
Date: Monday, December 15, 2008	Sheet 4 of 33

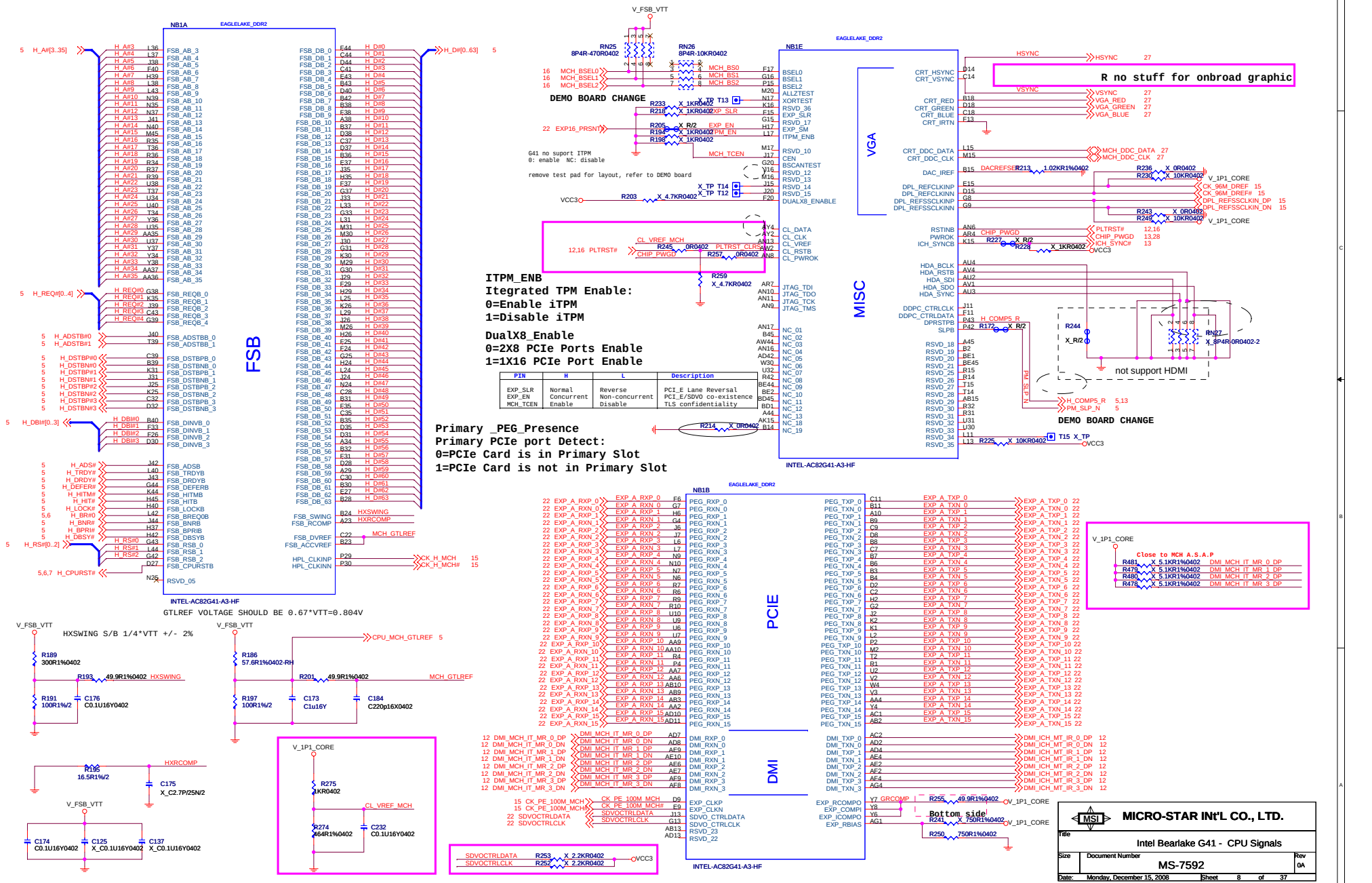

CPU SIGNAL BLOCK
PULL HIGHT PULL DOWN
CPU1A
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH
VCC_SENSE
VSS_SENSE
VID[0..7]
H_A#[3..35]
H_DBI#[0..3]
H_D#[0..63]
VTT_OUT_RIGHT
R75
680R1%0402
R188
X_0R0402
CPU_MCH_GTLREF
H_BPM#[0..4]
H_REQ#[0..4]
H_TESTHI12
DPSLP#
Kentsfield
R162
51R0402
V_FSB_VTT
R161
51R0402
R87
X_130R1%0402
VTT_OUT_LEFT
R139
X_51R0402
CK_H_CPU#
CK_H_CPU
H_RS#[0..2]
H_BR#0
H_COMP5_R
R117
X_R/2
R125
X_49.9R1%0402
R163
49.9R1%0402
RN8
8P4R-49.9R1%-1
H_ADSTB#1
H_ADSTB#0
H_DSTBP#3
H_DSTBP#2
H_DSTBP#1
H_DSTBP#0
H_DSTBN#3
H_DSTBN#2
H_DSTBN#1
H_DSTBN#0
H_NMI
H_INTR
R124
X_0R0402
R86
X_R/2
R95
X_1KR0402
R96
X_51R0402
RN4
8P4R-680R0402-RH
RN3
8P4R-680R0402-RH
RN5
8P4R-51R0402
RN6
8P4R-51R0402
RN7
8P4R-51R0402
RN9
8P4R-51R0402
C68
C0.1u16Y0402
DEMO circuit DPSLP# pull high
R132
51R0402
R127
51R0402
R113
49.9R1%0402
C70
X_C0.1u16Y0402
R135
X_51R0402
R90
X_0R0402
VRM_HOT
MICRO-STAR INT'L CO.,LTD
MS-7592
LGA775 - Signal
Rev 1.1
Date: Monday, December 15, 2008
Sheet 5 of 33

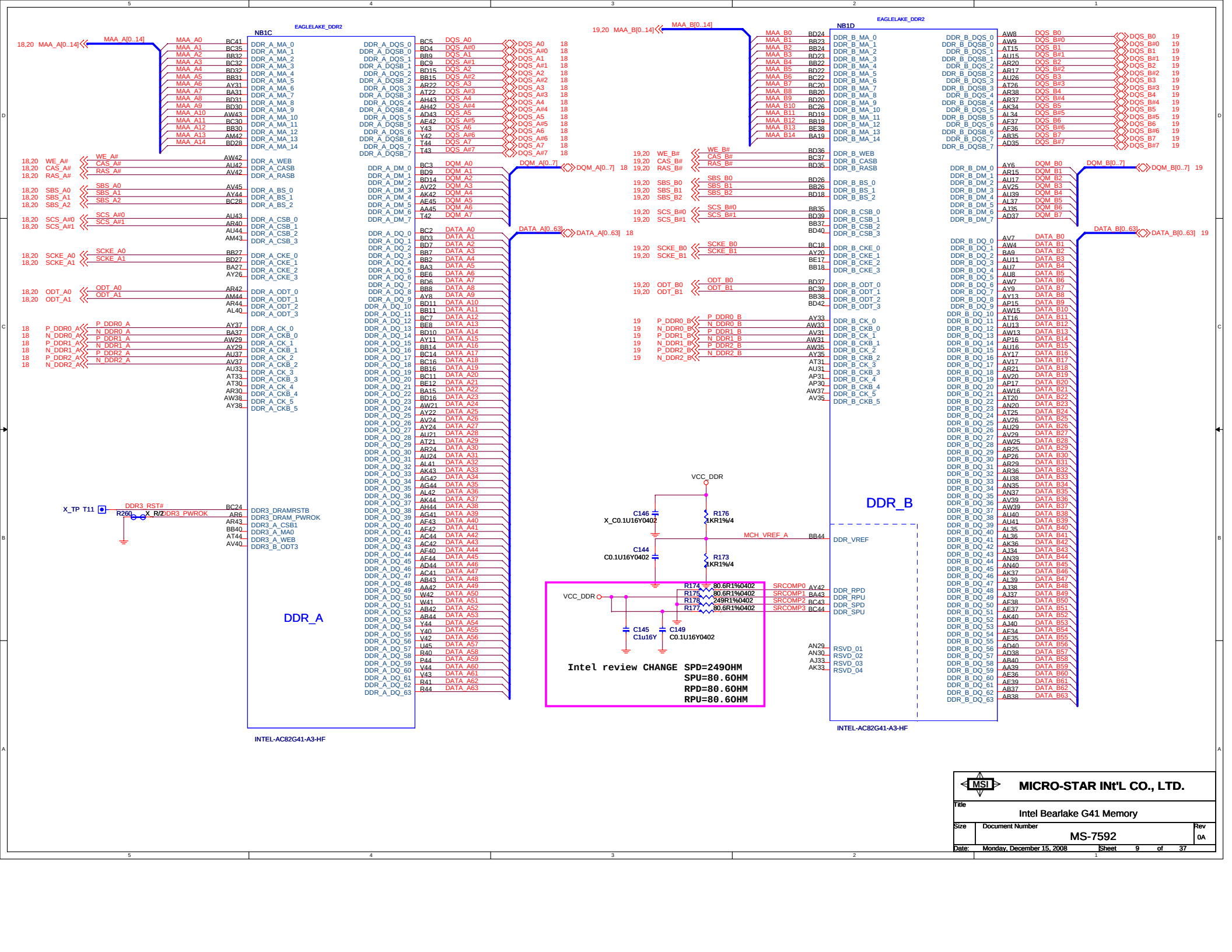

CPU1B
VCCP
VCC
VCCA
VSSA
VCCPLL
VCC-IOPLL
VTT
VTTPWRGD
RSVD#F29
H_VCCA
H_VSSA
H_VCCPLL
VTT_PWG
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_SEL
V_FSB_VTT
C135 C10u10Y0805
C132 X_C10u10Y0805
CAPS FOR FSB GENERIC
*GTLREF VOLTAGE SHOULD BE 0.67 * VTT = 0.8V (At VTT=1.2V)
R108 57.6R1%0402-RH
R110 100R1%0402
R107 100R1%/2
C62 C1u16Y
C66 X_C220p50N0402
CPU_GTLREF0 5
R120 X_0R0402 CPU_GTL_REF
R116 49.9R1%0402-RH
R126 10R1%0402
R123 100R1%/2
C71 C1u16Y
C75 X_C220p50N0402
CPU_GTLREF1 5
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS
L2 X_10u100mA_0805-RH
CP1
CP2
C108 C1u16Y
C113 C10u10Y0805
C116 X_C10u10Y0805
C117 X_C1u16Y
C130 C10u10Y0805
V_1P5_CORE
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH
PLACE AT CPU END OF ROUTE
R98 130R1%0402
R106 62R0402
R137 62R0402
R118 X_100R0402
R138 62R0402
H_PROCHOT#
H_IERR#
H_CPURST#
H_PWRGD
H_BR#0
5VSB
R85 10KR0402
R84 X_10KR0402
C57 C1u16Y0402
Address:60h
U5
UP6262M8_SOT23-8-RH
SMBCLK_ISO 13,15,17,18,22,28
SMBDATA_ISO 13,15,17,18,22,28
DIMM_MEM_REF 18,19
CPU_VRM_REF 30
reserved
VTT_PWRGOOD
R88 680R0402-RH
R79 1KR0402
C54 X_C1u16Y
Q11 N-MMBT3904_NL_SOT23
VID_GD# 28,30
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
MICRO-STAR INT'L CO.,LTD
MS-7592
Size Custom
Document Description LGA775 - Power
Rev 1.1
Date: Monday, December 15, 2008
Sheet 6 of 33

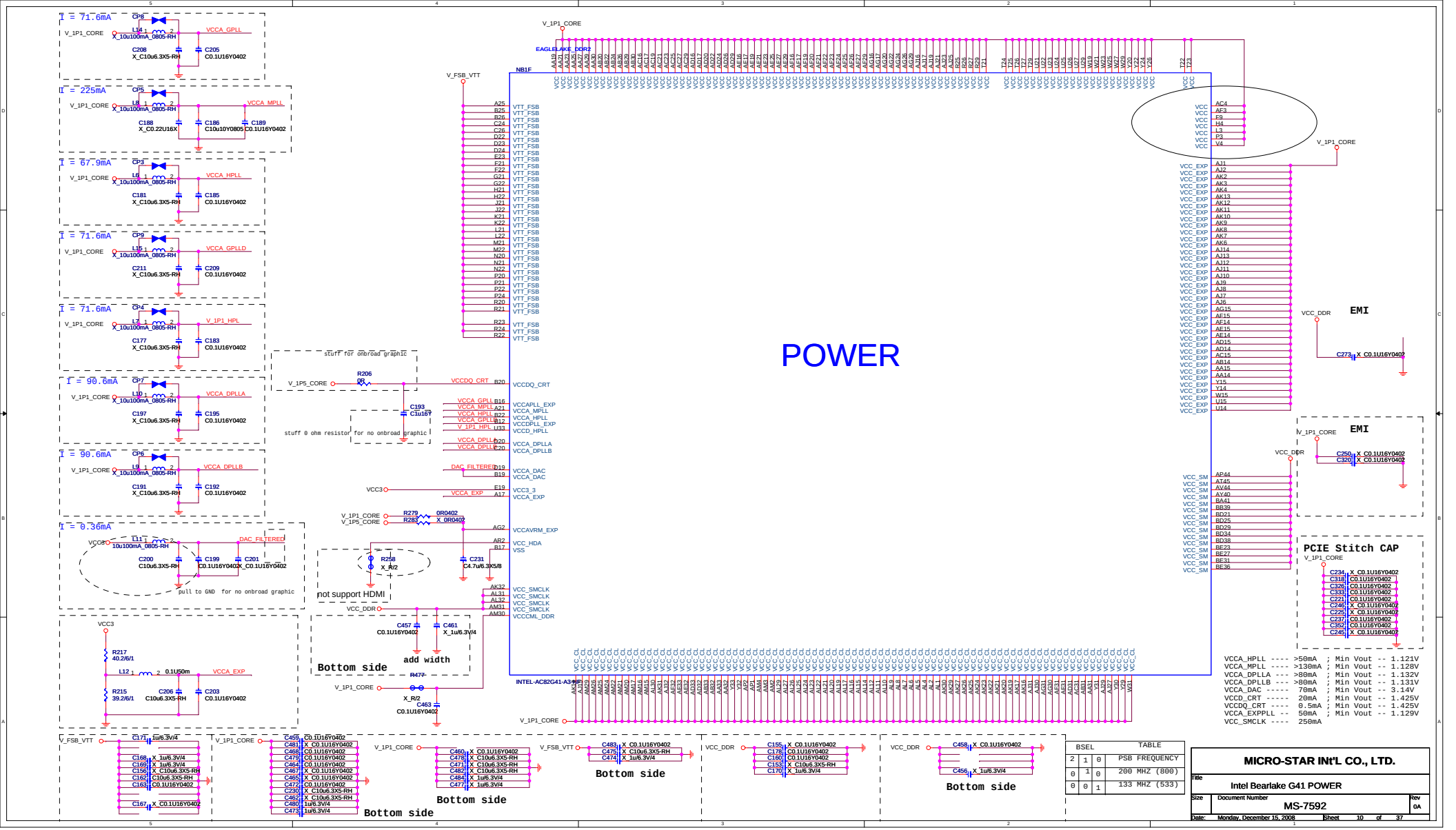


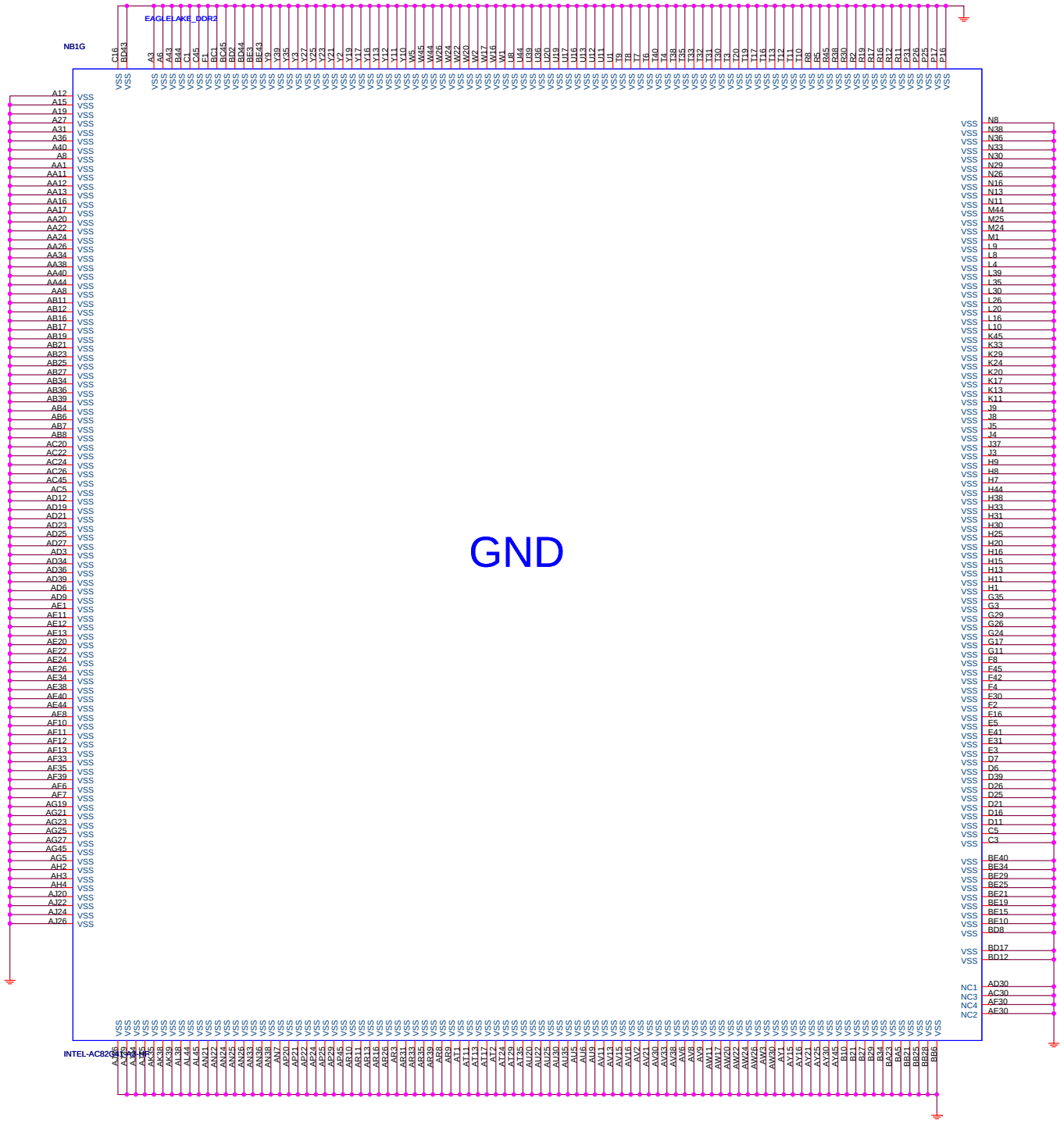
	MSID1	MSID0
05 Per FMB	0	0
05 Value FMB	0	1

MICRO-STAR INT'L CO.,LTD		
MS-7592		
Size: Custom	Document Description: LGA775 - GND	Rev: 1.1
Date: Monday, December 15, 2008	Sheet 7 of 33	

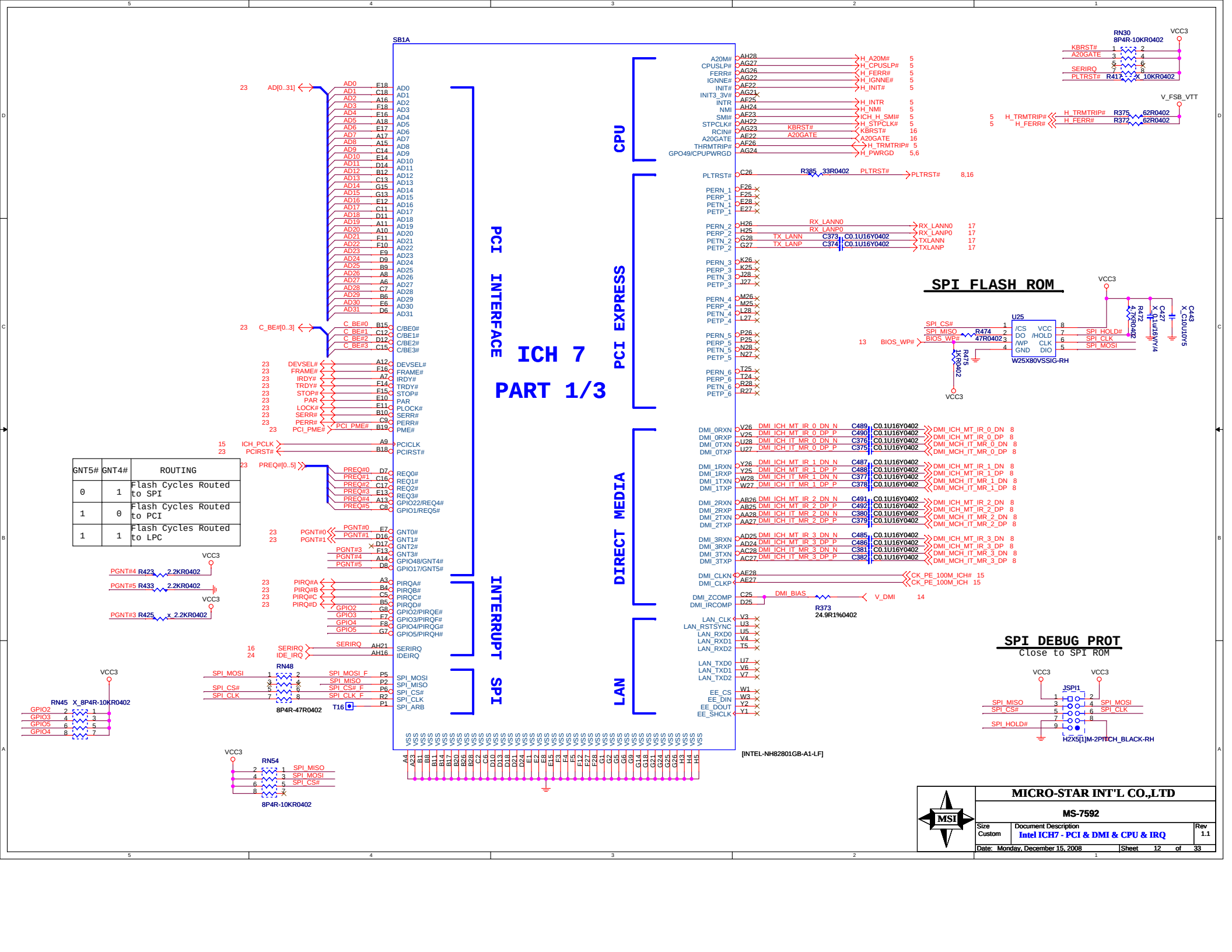

NB1A
EAGLELAKE_DDR2
FSB
INTEL-AC82G41-A3-HF
GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.804V
V_FSB_VTT
HXSWING S/B 1/4*VTT +/- 2%
R189 300R1%0402
R193 49.9R1%0402 HXSWING
R191 100R1%/2
C176 C0.1U16Y0402
R186 57.6R1%0402-RH
R201 49.9R1%0402
MCH_GTLREF
R197 100R1%/2
C173 C1u16Y
C184 C220p16X0402
CPU_MCH_GTLREF
R199 16.5R1%/2
HXRCOMP
C175 X_C2.7P25N/2
C174 C0.1U16Y0402
C125 X_C0.1U16Y0402
C137 X_C0.1U16Y0402
V_1P1_CORE
R275 1KR0402
CL_VREF_MCH
R274 464R1%0402
C232 C0.1U16Y0402
RN25 8P4R-470R0402
RN26 8P4R-10KR0402
DEMO BOARD CHANGE
X_TP T13
X_TP T14
X_TP T12
R233 X_1KR0402
R218 X_1KR0402
R205 X_R/2
R194 X_1KR0402
R198 X_1KR0402
R203 X_4.7KR0402
G41 no suport ITPM
0: enable NC: disable
remove test pad for layout, refer to DEMO board
ITPM_ENB
Itegrated TPM Enable:
0=Enable iTPM
1=Disable iTPM
DualX8_Enable
0=2X8 PCIe Ports Enable
1=1X16 PCIe Port Enable
PIN | H | L | Description
EXP_SLR | Normal | Reverse | PCI_E Lane Reversal
EXP_EN | Concurrent | Non-concurrent | PCI_E/SDVO co-existence
MCH_TCEN | Enable | Disable | TLS confidentiality
Primary _PEG_Presence
Primary PCIe port Detect:
0=PCIe Card is in Primary Slot
1=PCIe Card is not in Primary Slot
R214 X_0R0402
R259 X_4.7KR0402
R245 0R0402
R257 0R0402
CL_VREF_MCH
CHIP_PWGD
PLTRST_CLRSV
NB1E
VGA
MISC
R no stuff for onboard graphic
DACREFSET
R213 1.02KR1%0402
R236 X_0R0402
R230 X_10KR0402
R243 X_0R0402
R249 X_10KR0402
R227 X_R/2
R228 X_1KR0402
R172 X_R/2
R244 X_R/2
RN27 X_8P4R-0R0402-2
not support HDMI
DEMO BOARD CHANGE
R225 X_10KR0402
T15 X_TP
NB1B
PCIE
DMI
R255 49.9R1%0402
R241 X_750R1%0402
R250 750R1%0402
Bottom side
R481 X_5.1KR1%0402
R479 X_5.1KR1%0402
R480 X_5.1KR1%0402
R478 X_5.1KR1%0402
Close to MCH A.S.A.P
SDVOCTRLDATA
SDVOCTRLCLK
R253 X_2.2KR0402
R252 X_2.2KR0402
MICRO-STAR INt'L CO., LTD.
Intel Bearlake G41 - CPU Signals
MS-7592
Rev 0A
Date: Monday, December 15, 2008
Sheet 8 of 37


EAGLELAKE_DDR2
NB1C
DDR_A
INTEL-AC82G41-A3-HF
EAGLELAKE_DDR2
NB1D
DDR_B
INTEL-AC82G41-A3-HF
VCC_DDR
R176 1KR1%/4
R173 1KR1%/4
MCH_VREF_A
R174 80.6R1%0402
R175 80.6R1%0402
R178 249R1%0402
R177 80.6R1%0402
SRCOMP0
SRCOMP1
SRCOMP2
SRCOMP3
C145 C1u16Y
C149 C0.1U16Y0402
Intel review CHANGE SPD=249OHM
SPU=80.6OHM
RPD=80.6OHM
RPU=80.6OHM
MSI
MICRO-STAR INt'L CO., LTD.
Title
Intel Bearlake G41 Memory
Size
Document Number
MS-7592
Rev
0A
Date: Monday, December 15, 2008
Sheet 9 of 37

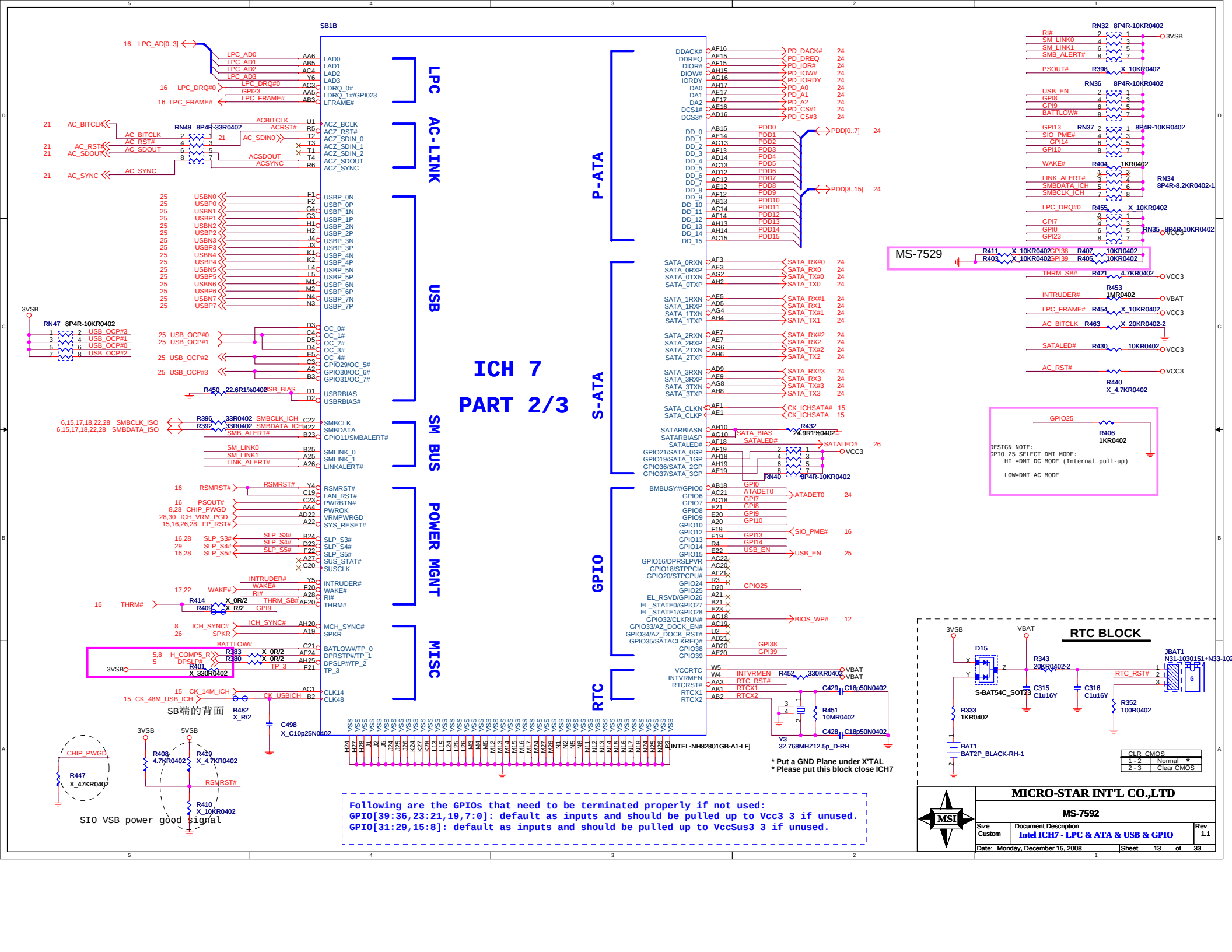

POWER
I = 71.6mA
I = 225mA
I = 67.9mA
I = 71.6mA
I = 71.6mA
I = 90.6mA
I = 90.6mA
I = 0.36mA
V_1P1_CORE
EAGLELAKE_DDR2
NB1F
V_FSB_VTT
VCCA_GPLL
VCCA_MPLL
VCCA_HPLL
VCCA_GPLLD
V_1P1_HPL
VCCA_DPLLA
VCCA_DPLLB
DAC_FILTERED
VCC3
VCCA_EXP
V_1P5_CORE
VCCDQ_CRT
VCCAVRM_EXP
VCC_HDA
VCC_SMCLK
VCCCML_DDR
not support HDMI
stuff for onbroad graphic
stuff 0 ohm resistor for no onbroad graphic
pull to GND for no onbroad graphic
add width
Bottom side
INTEL-AC82G41-A3
EMI
PCIE Stitch CAP
VCC_DDR
VCC_SM
VCC_EXP
VCCA_HPLL ---- >50mA ; Min Vout -- 1.121V
VCCA_MPLL ---- >130mA ; Min Vout -- 1.128V
VCCA_DPLLA ---- >80mA ; Min Vout -- 1.132V
VCCA_DPLLB ---- >80mA ; Min Vout -- 1.131V
VCCA_DAC ----- 70mA ; Min Vout -- 3.14V
VCCD_CRT ----- 20mA ; Min Vout -- 1.425V
VCCDQ_CRT ---- 0.5mA ; Min Vout -- 1.425V
VCCA_EXPPLL -- 50mA ; Min Vout -- 1.129V
VCC_SMCLK ---- 250mA
BSEL TABLE
2 1 0 PSB FREQUENCY
0 1 0 200 MHZ (800)
0 0 1 133 MHZ (533)
MICRO-STAR INt'L CO., LTD.
Intel Bearlake G41 POWER
Document Number MS-7592
Rev 0A
Date: Monday, December 15, 2008
Sheet 10 of 37

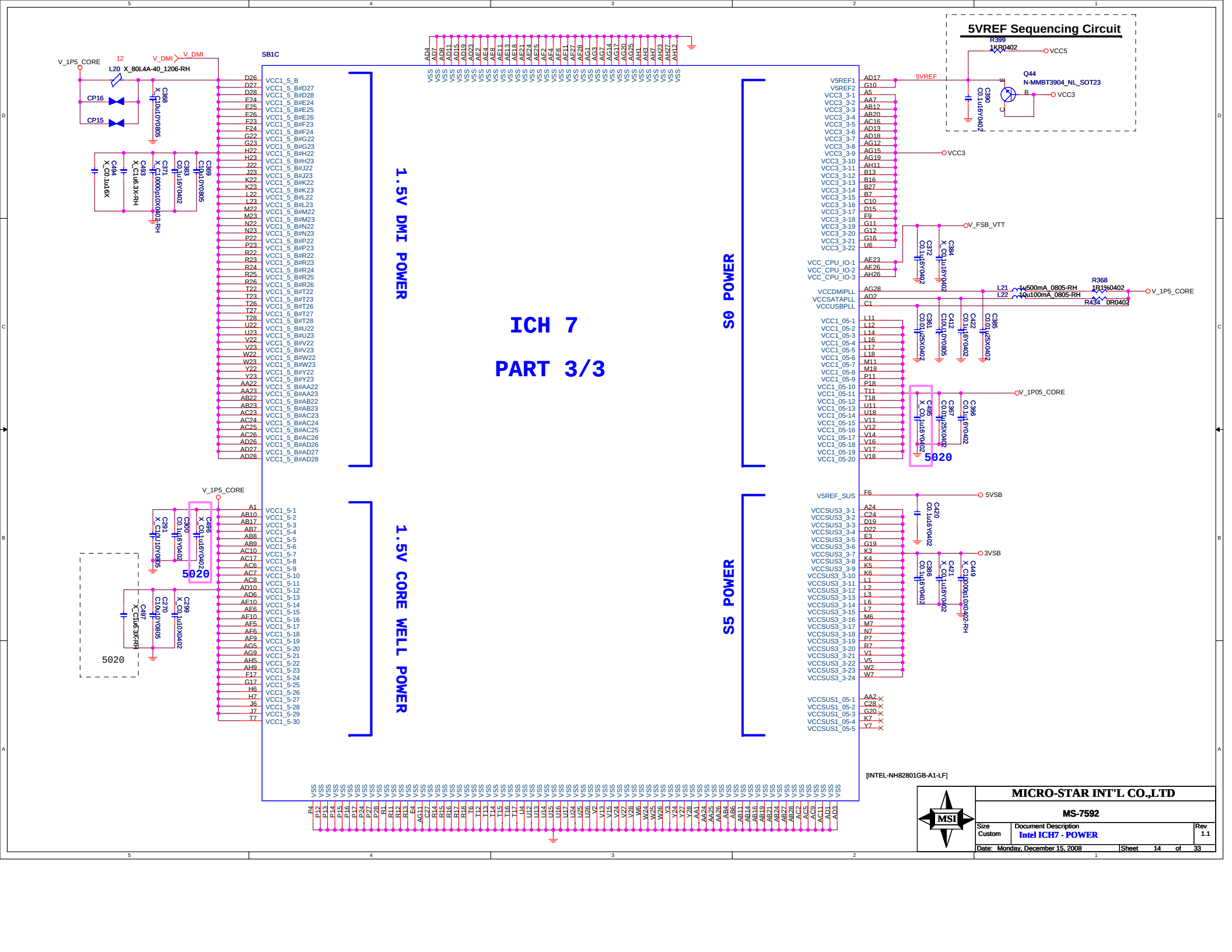


MSI	MICRO-STAR INt'L CO., LTD.
Title	Intel Bearlake G41 GND
Size	Document Number: MS-7592
Rev	0A
Date:	Monday, December 15, 2008
Sheet	11 of 37

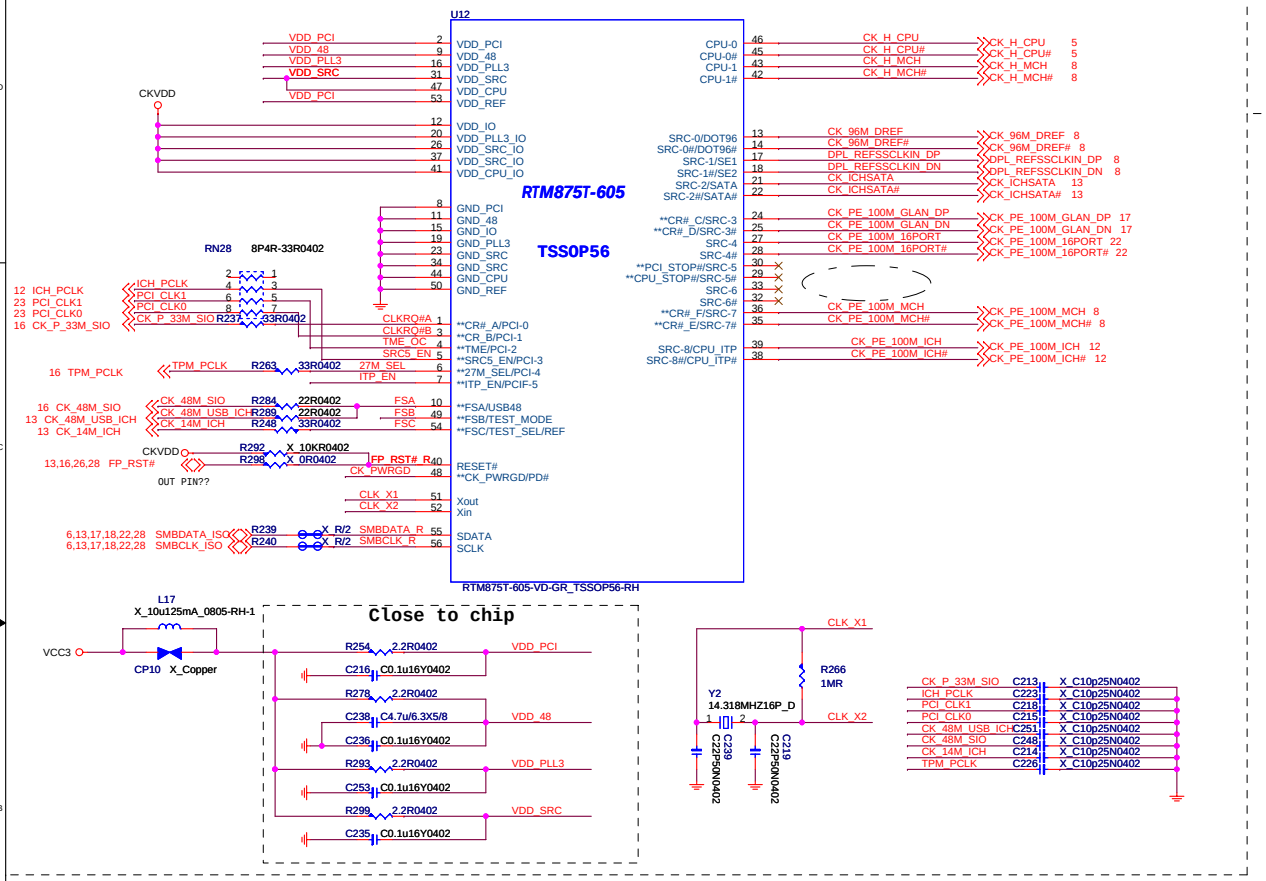


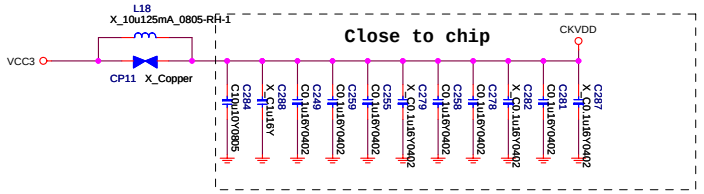
GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC


ICH 7
PART 2/3
LPC
AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-ATA
GPIO
RTC
SB1B
[INTEL-NH82801GB-A1-LF]
MS-7529
RTC BLOCK
SB端的背面
SIO VSB power good signal
* Put a GND Plane under X'TAL
* Please put this block close ICH7
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
MICRO-STAR INT'L CO.,LTD
MS-7592
Intel ICH7 - LPC & ATA & USB & GPIO
Rev 1.1
Date: Monday, December 15, 2008
Sheet 13 of 33

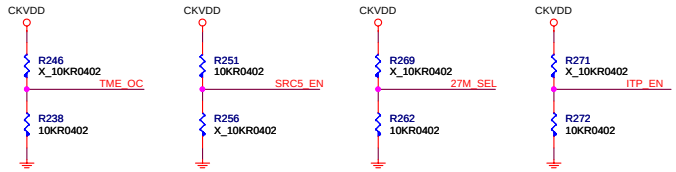

ICH 7
PART 3/3
1.5V DMI POWER
1.5V CORE WELL POWER
S0 POWER
S5 POWER
SB1C
5VREF Sequencing Circuit
R399 1KR0402
VCC5
Q44 N-MMBT3904_NL_SOT23
VCC3
5VREF
V_1P5_CORE
V_1P05_CORE
V_FSB_VTT
5VSB
3VSB
L20 X_80L4A-40_1206-RH
L21 1u500mA_0805-RH
L22 10u100mA_0805-RH
R368 1R1%0402
R434 0R0402
5020
[INTEL-NH82801GB-A1-LF]
MICRO-STAR INT'L CO.,LTD
MS-7592
Intel ICH7 - POWER
Rev 1.1
Date: Monday, December 15, 2008
Sheet 14 of 33

Clock Generator - RTM875T-605

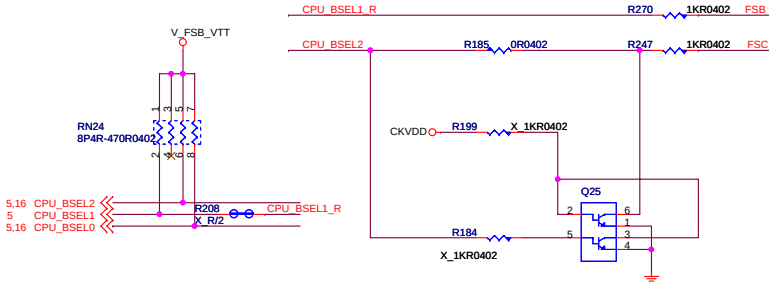




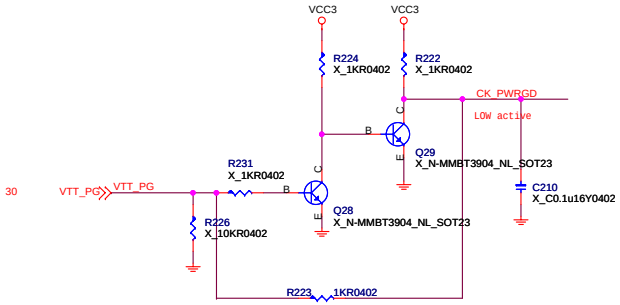
STRAPPING RESISTOR

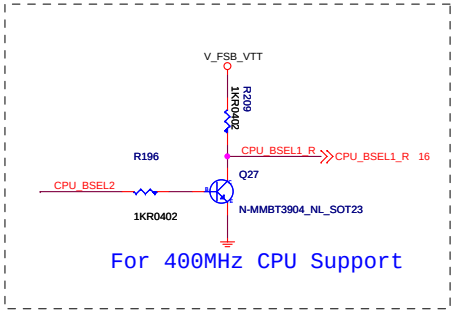


	0	1
TME_OC	Normal Run	No Overclocking
SRC5_EN	Pin29/30 is PCI STOP/CPU STOP	Pin29/30 is SRC 5
27M_SEL	Pin17/18 is SRC 1	Pin17/18 is 27MHz
ITP_EN	Pin38/39 is SRC 8	Pin38/39 is CPUITP



Clock Generator Power Good Block

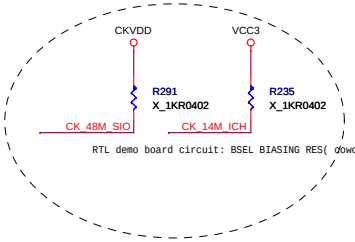


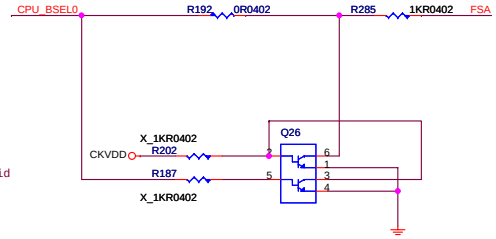


CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid



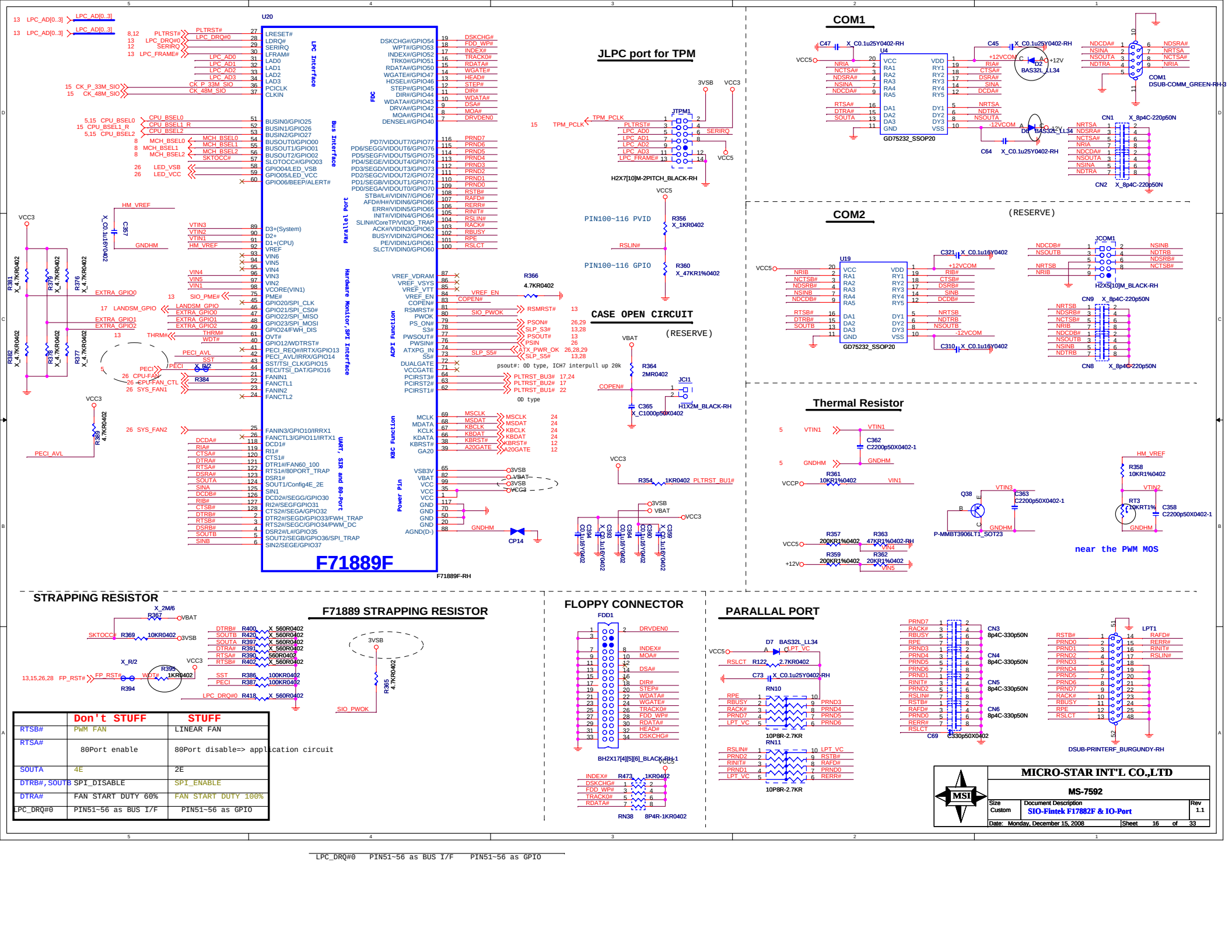


MICRO-STAR INT'L CO.,LTD

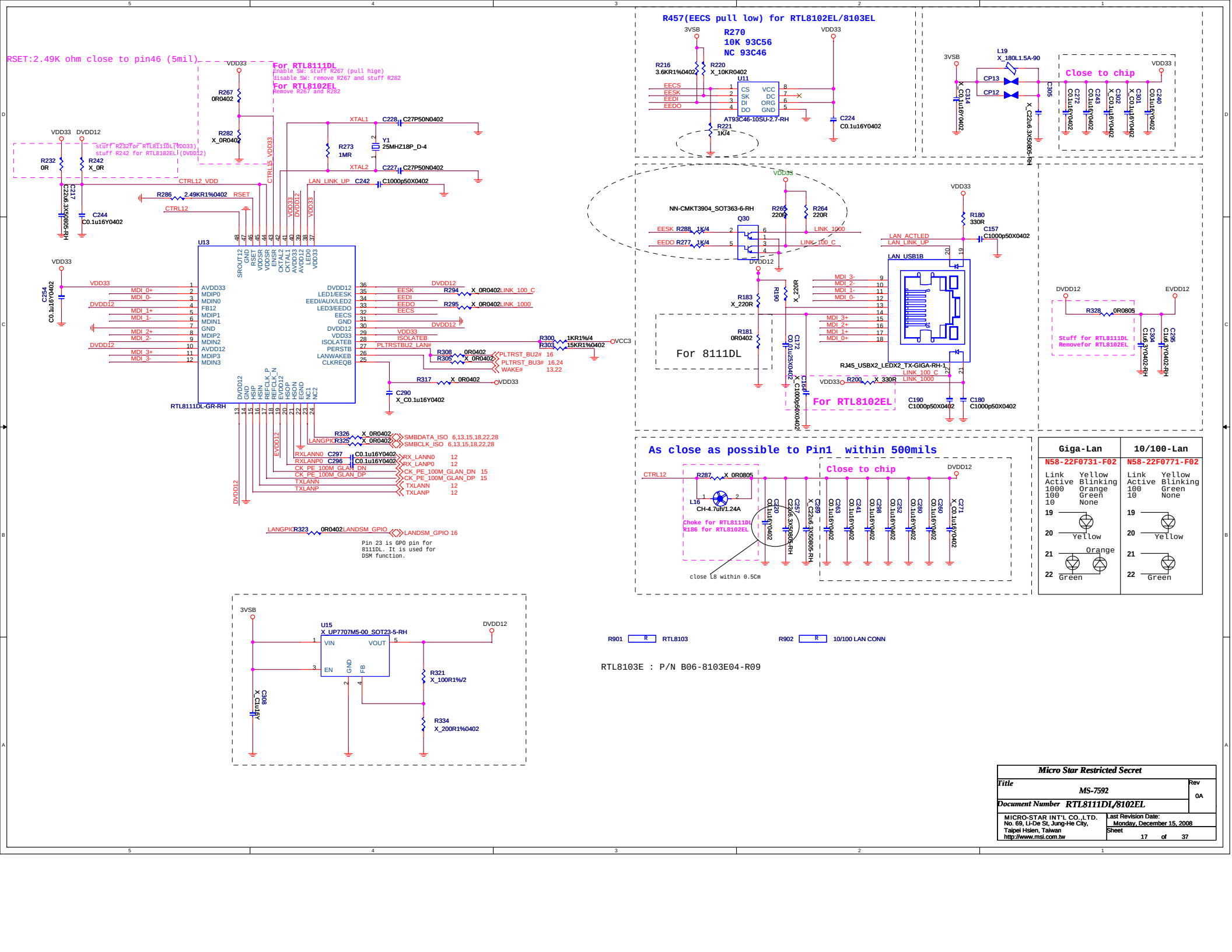
MS-7592

Size	Document Description	Rev
Custom	CLK-RTM 875T-605	0A

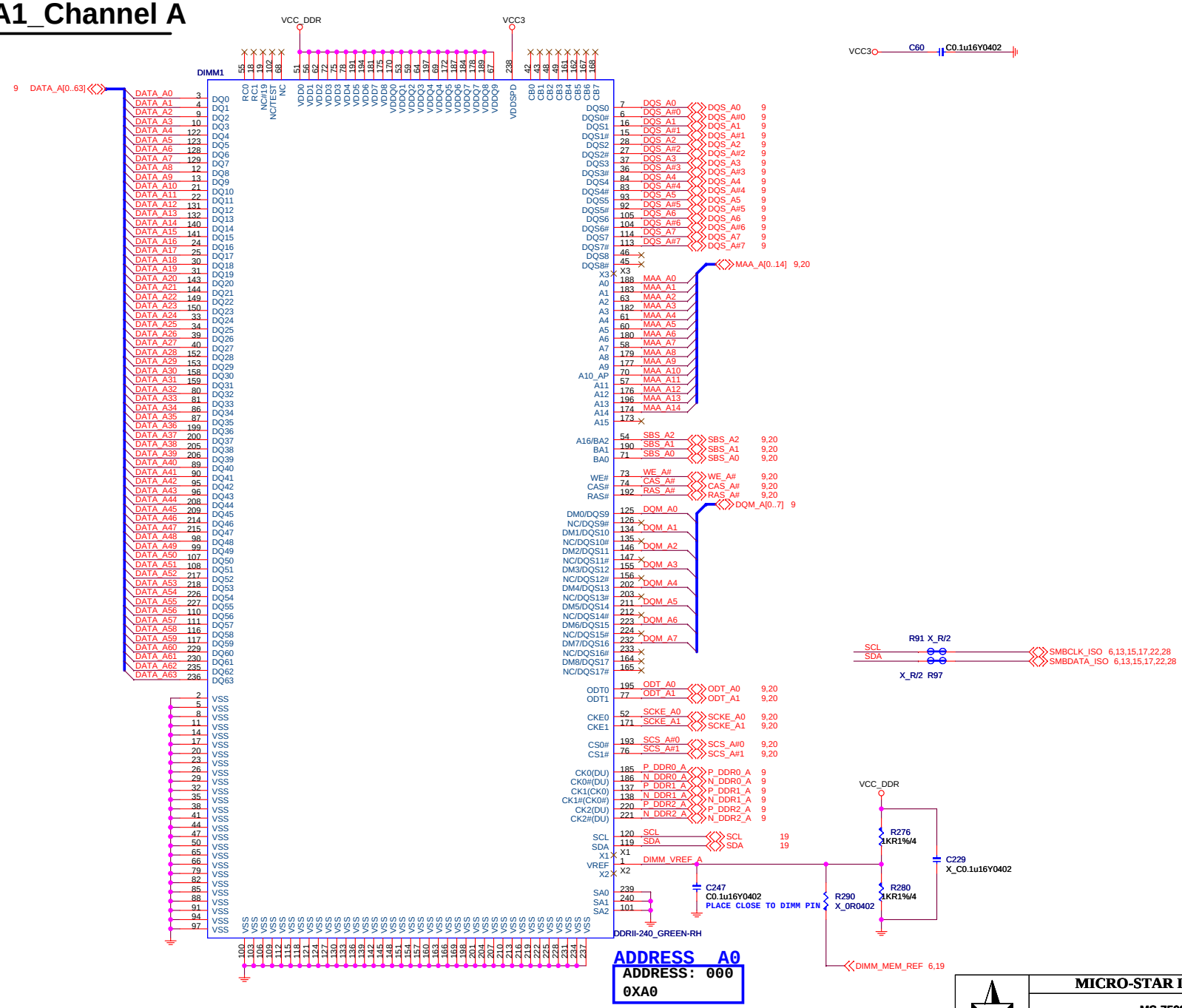
Date: Monday, December 15, 2008 Sheet 15 of 37



LPC_DRQ#0 PIN51~56 as BUS I/F PIN51~56 as GPIO

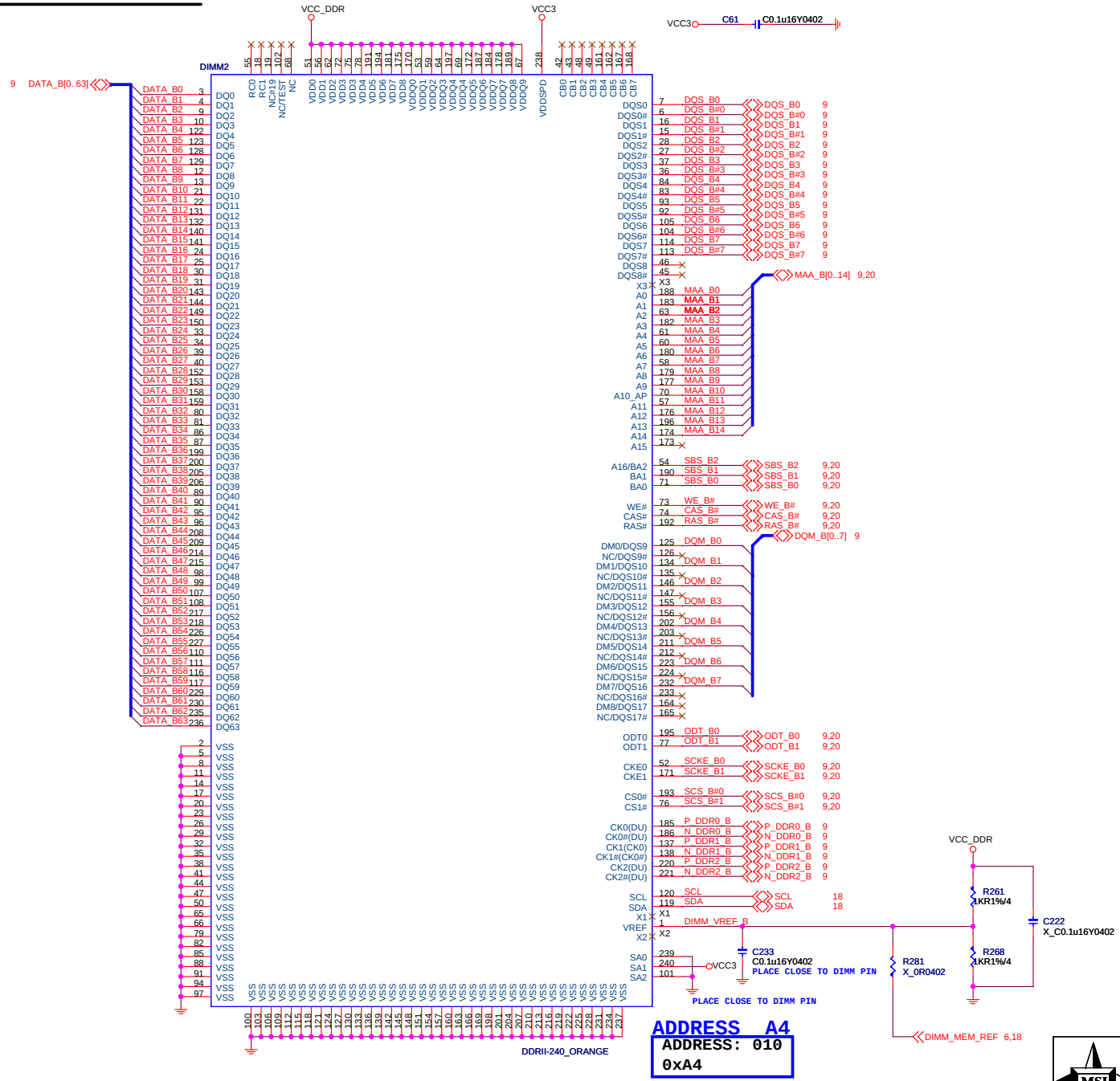

RSET:2.49K ohm close to pin46 (5mil)
For RTL8111DL
Enable SW: stuff R267 (pull hige)
disable SW: remove R267 and stuff R282
For RTL8102EL
Remove R267 and R282
stuff R232 for RTL8111DL(VDD33)
stuff R242 for RTL8102EL(DVDD12)
R457(EECS pull low) for RTL8102EL/8103EL
R270
10K 93C56
NC 93C46
AT93C46-10SU-2.7-RH
Close to chip
NN-CMKT3904_SOT363-6-RH
LAN_USB1B
RJ45_USBX2_LEDX2_TX-GIGA-RH-1
For 8111DL
For RTL8102EL
As close as possible to Pin1 within 500mils
Choke for RTL8111DL
#186 for RTL8102EL
close L8 within 0.5Cm
RTL8111DL-GR-RH
Pin 23 is GPO pin for
8111DL. It is used for
DSM function.
U15
X_UP7707M5-00_SOT23-5-RH
Stuff for RTL8111DL
Removefor RTL8102EL
Giga-Lan
N58-22F0731-F02
10/100-Lan
N58-22F0771-F02
Link Active 1000 100 10
Blinking Orange Green None
Yellow
Orange
Green
R901 R RTL8103
R902 R 10/100 LAN CONN
RTL8103E : P/N B06-8103E04-R09
Micro Star Restricted Secret
Title MS-7592
Rev 0A
Document Number RTL8111DL/8102EL
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date: Monday, December 15, 2008
Sheet 17 of 37

DDRII DIMM_A1_Channel A



MICRO-STAR INT'L CO.,LTD	
MS-7592	
Size: Custom	Document Description: DDR II DIMM A
Rev: 1.0	
Date: Monday, December 15, 2008	Sheet 18 of 37

DDRII DIMM_B1_Channel B



MICRO-STAR INT'L CO.,LTD

MS-7592

Size	Document Description	Rev
Custom	DDR II DIMM B	1.0

Date: Monday, December 15, 2008 Sheet 19 of 37

CHANNEL A V_SM_VTT DECOULPING CAPS

VTT_DDR
C96 X_C4.7u6.3X5
C114 X_C4.7u6.3X5

VTT_DDR
C134 X_C0.1u16Y0402
C120 X_C0.1u16Y0402
C105 X_C0.1u16Y0402

VCC_DDR
C142 X_C0.1u16Y0402

VCC5 12VIN
C207 X_C0.1u16Y0402
C56 X_C0.1u16Y0402

CHANNEL B V_SM_VTT DECOULPING CAPS

VTT_DDR
C138 C4.7u6.3X5

VTT_DDR
C103 X_C0.1u16Y0402
C99 X_C0.1u16Y0402
C129 X_C0.1u16Y0402
C106 X_C0.1u16Y0402

EMI 10/29

VCC_DDR VTT_DDR
C124 X_C0.1U16Y0402
C141 X_C0.1U16Y0402
C111 X_C0.1U16Y0402
C97 X_1u/6.3V/4
C102 X_1u/6.3V/4

VTT_DDR

RN18 8P4R-33R0402
MAA_A4 MAA_A3 MAA_A2 MAA_A1

RN20 8P4R-33R0402
MAA_A7 MAA_A8 MAA_A5 MAA_A6

9,18 SBS_A2

RN22 8P4R-33R0402
MAA_A12 MAA_A11 MAA_A9

9,18 RAS_A#
9,18 WE_A#
9,18 CAS_A#

RN15 8P4R-33R0402
RAS_A# WE_A# CAS_A# MAA_A13

MAA_A14 R165 33R0402

RN17 8P4R-33R0402
MAA_A0 SBS_A1 MAA_A10 SBS_A0

9,18 SBS_A1
9,18 SBS_A0

RN13 8P4R-43R0402
ODT_A1 SCS_A#1 ODT_A0 SCS_A#0

9,18 ODT_A1
9,18 SCS_A#1
9,18 ODT_A0
9,18 SCS_A#0

SCKE_A0 R167 43R0402
SCKE_A1 R170 43R0402

9,18 SCKE_A0
9,18 SCKE_A1

change RN

9,18 MAA_A[0..14]

VTT_DDR

RN19 8P4R-33R0402
MAA_B4 MAA_B3 MAA_B1 MAA_B2

RN21 8P4R-33R0402
MAA_B7 MAA_B8 MAA_B6 MAA_B5

9,19 SBS_B2

RN23 8P4R-33R0402
MAA_B12 MAA_B11 MAA_B9

9,19 RAS_B#
9,19 WE_B#
9,19 CAS_B#

RN14 8P4R-33R0402
RAS_B# WE_B# CAS_B# MAA_B13

MAA_B14 R166 33R0402

RN16 8P4R-33R0402
MAA_B0 SBS_B1 MAA_B10 SBS_B0

9,19 SBS_B1
9,19 SBS_B0

RN12 8P4R-43R0402
ODT_B1 SCS_B#1 SCS_B#0 ODT_B0

9,19 ODT_B1
9,19 SCS_B#1
9,19 SCS_B#0
9,19 ODT_B0

SCKE_B0 R171 43R0402
SCKE_B1 R169 43R0402

9,19 SCKE_B0
9,19 SCKE_B1

change RN

9,19 MAA_B[0..14]

VCC_DDR VCC_DDR
C140 X_C0.1u16Y0402
C92 X_C0.1u16Y0402

C476 X_C4.7u6.3X5
C276 X_1u/6.3V/4
C100 X_1u/6.3V/4
C85 X_1u/6.3V/4
C147 X_1u/6.3V/4
C182 X_1u/6.3V/4
C187 X_1u/6.3V/4
C469 X_1u/6.3V/4

VCC_DDR
C115 1u/6.3V/4
C104 X_1u/6.3V/4
C143 X_1u/6.3V/4
C470 X_1u/6.3V/4
C165 1u/6.3V/4
C112 X_1u/6.3V/4
C212 X_1u/6.3V/4

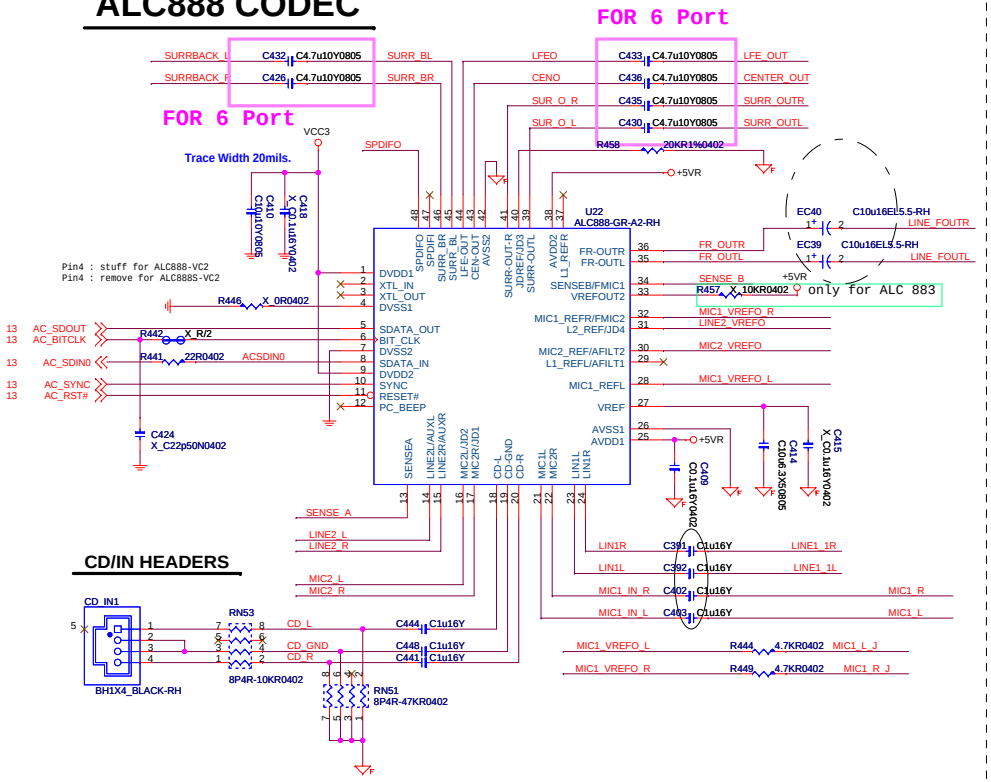
MICRO-STAR INT'L CO.,LTD

MS-7592

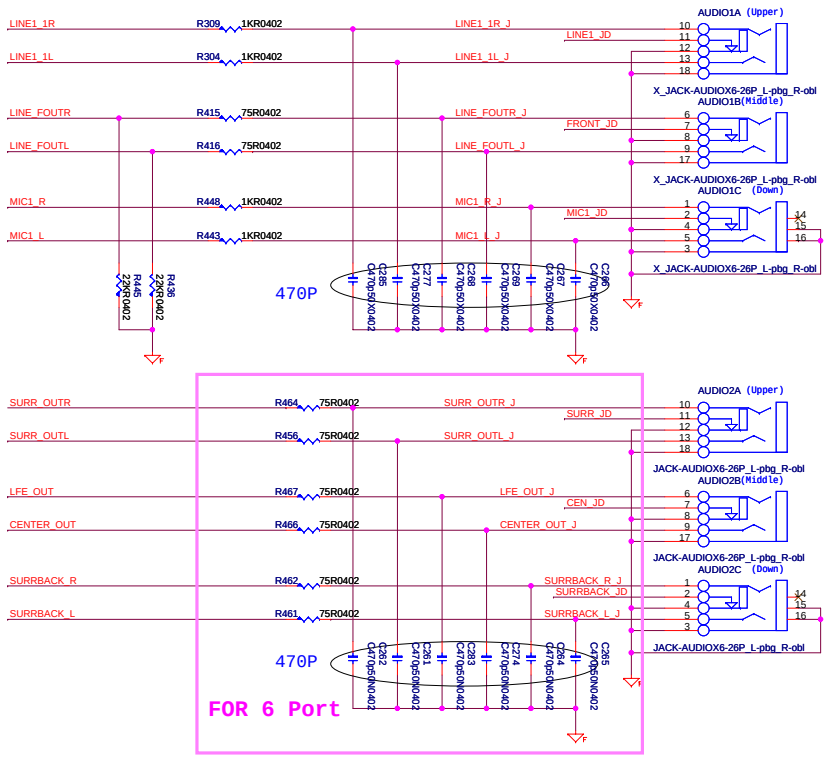
Size	Document Description	Rev
Custom	DDR II VTT DECOUPLING	1.0

Date: Monday, December 15, 2008 Sheet 20 of 37

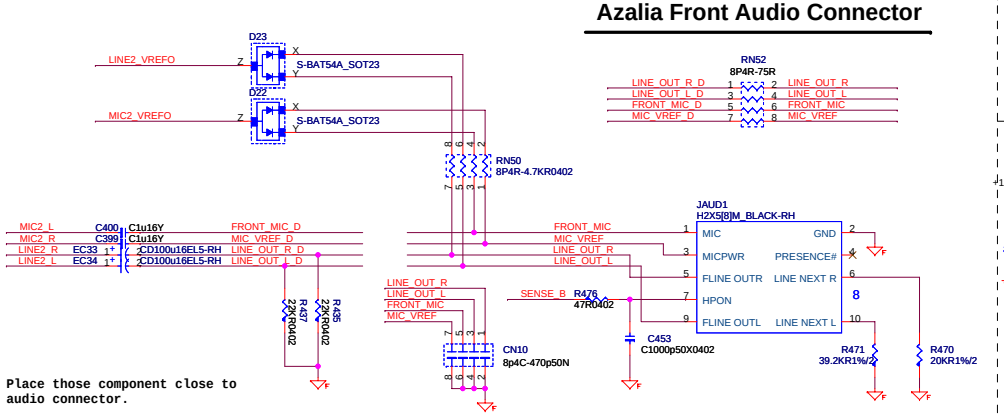
ALC888 CODEC



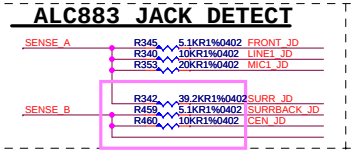
ALC888 JACK



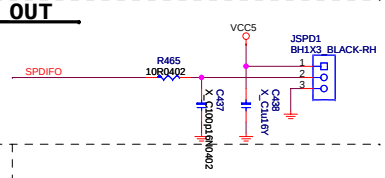
Azalia Front Audio Connector



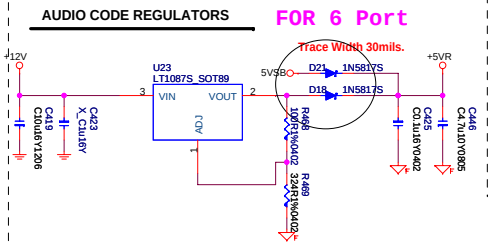
ALC883 JACK DETECT



SPDIF OUT

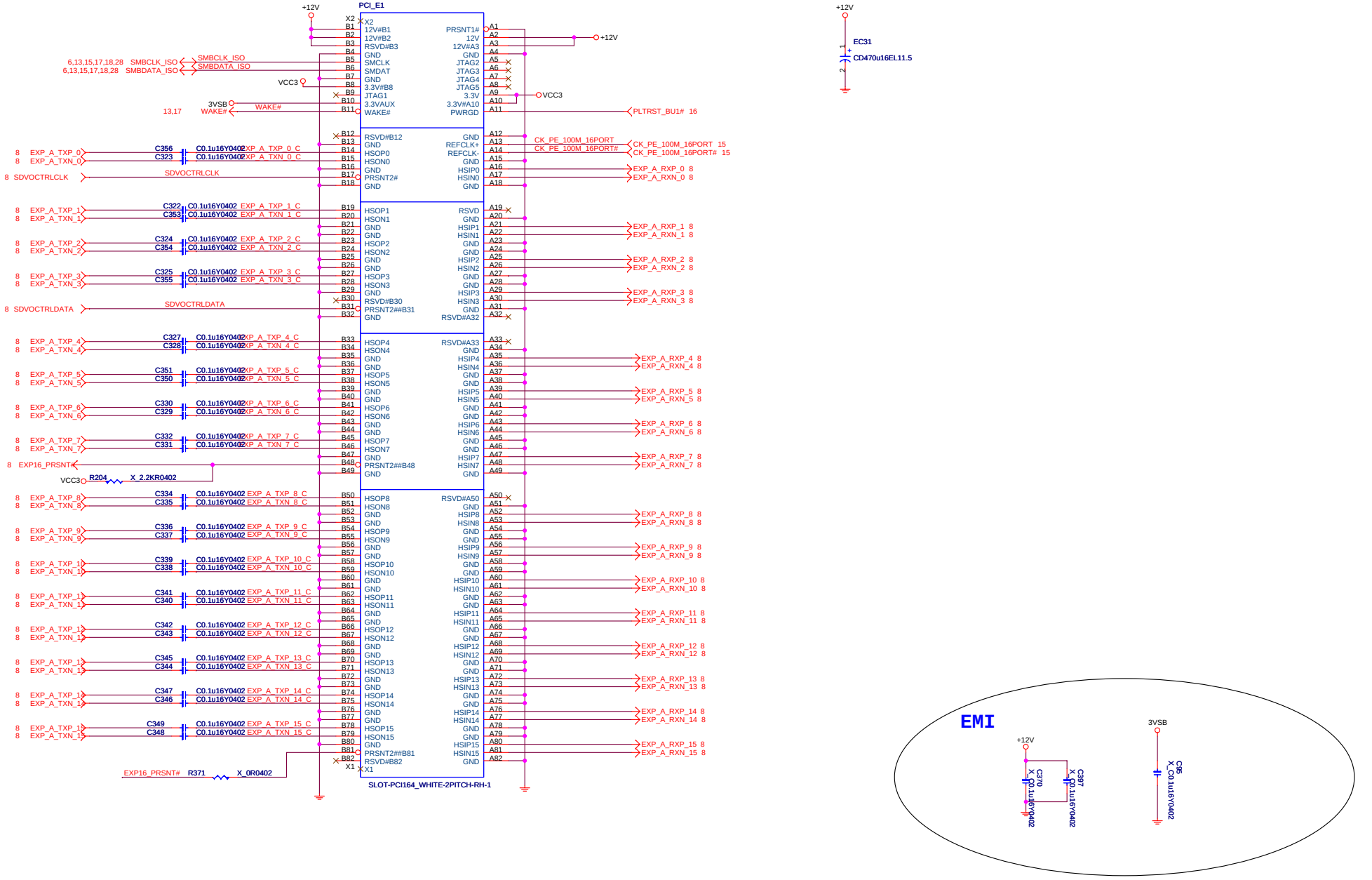


AUDIO CODE REGULATORS



MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7592		
Size: Custom	Document Description: 21 HD ALC888		Rev: 1.1
Date: Monday, December 15, 2008		Sheet 21 of 33	

PCIE X16 PORT

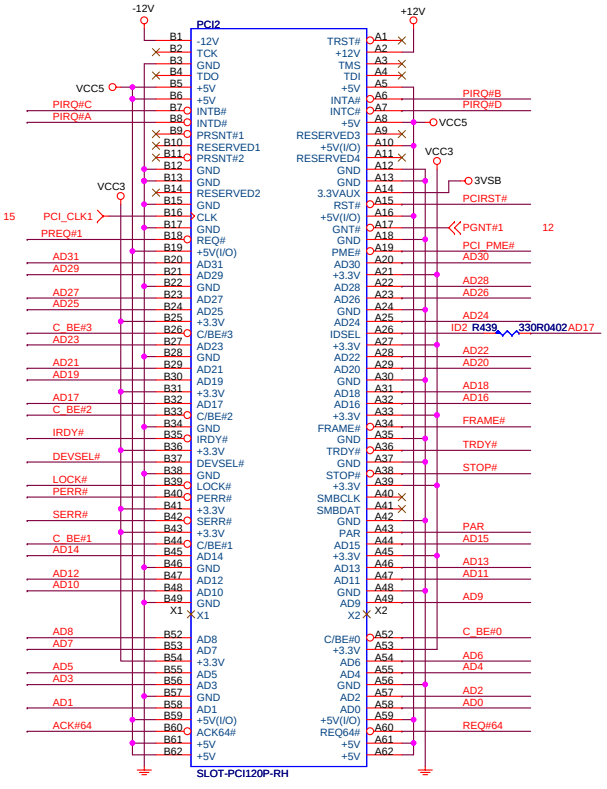


MICRO-STAR INT'L CO.,LTD	
MS-7592	
Size: Custom	Document Description: PCI EXPRESSX16&X1
Rev: 1.1	
Date: Monday, December 15, 2008	Sheet 22 of 33

PCI SLOT 1 (PCI VER: 2.2 COMPLY)

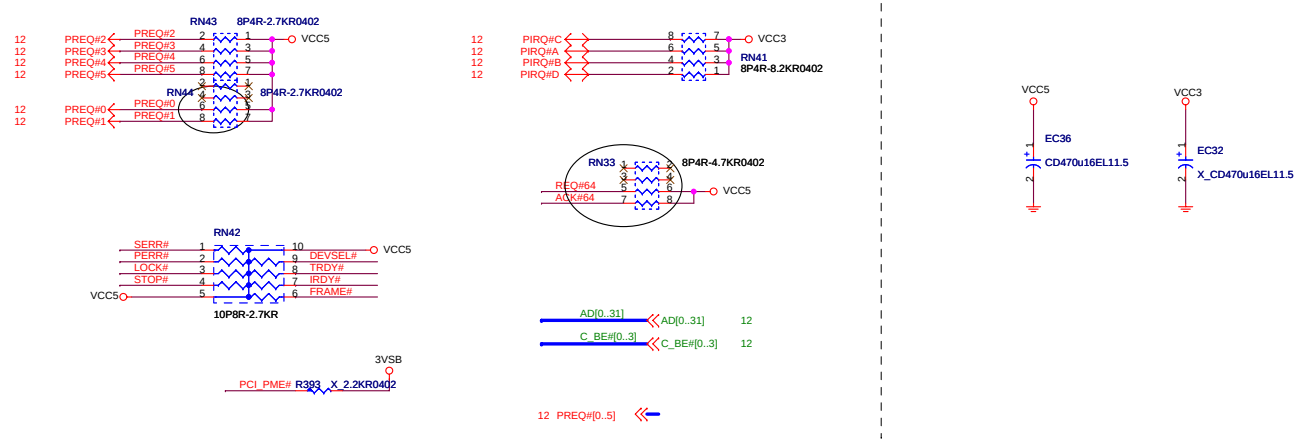
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



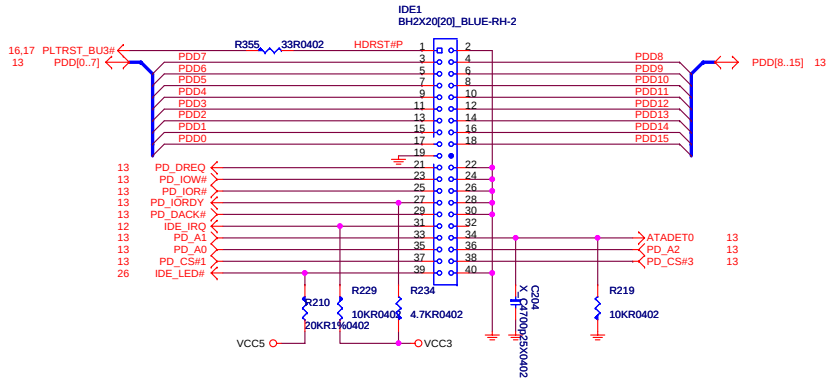
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS

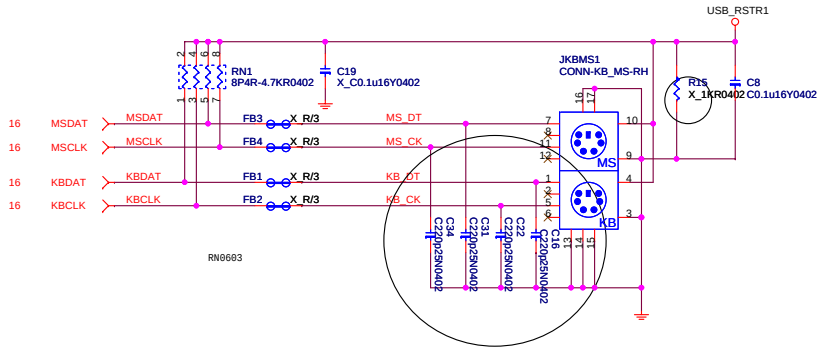


MICRO-STAR INT'L CO.,LTD		
MS-7592		
Size: Custom	Document Description: PCI Slot 1 &2	Rev: 1.1
Date: Monday, December 15, 2008	Sheet 23 of 33	

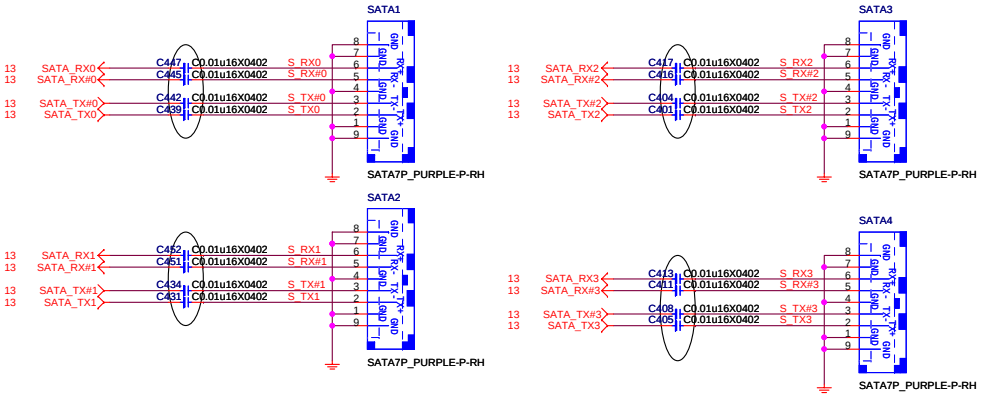
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK



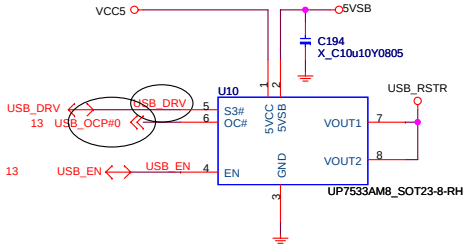
MICRO-STAR INT'L CO.,LTD

MS-7592

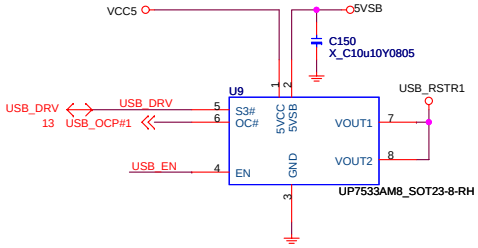
Size	Document Description	Rev
Custom	IDE & SATA Connectors	1.1

Date: Monday, December 15, 2008 Sheet 24 of 33

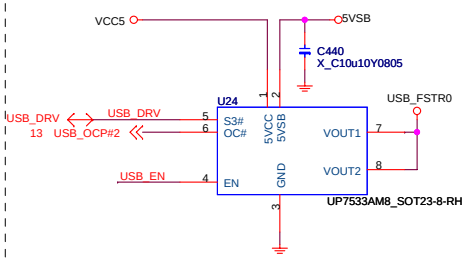
POWER CIRCUIT FOR USB PORT 0,1



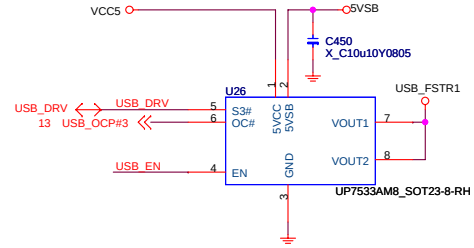
POWER CIRCUIT FOR USB PORT 2,3



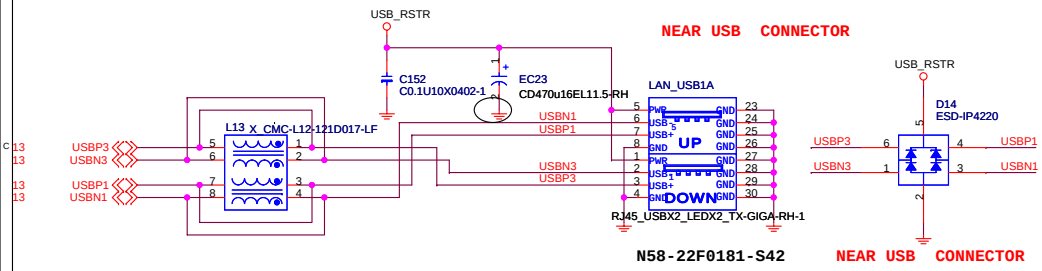
POWER CIRCUIT FOR USB PORT 4,5



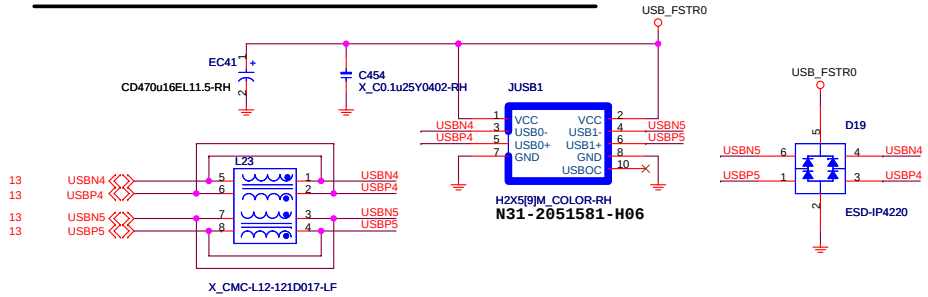
POWER CIRCUIT FOR USB PORT 6,7



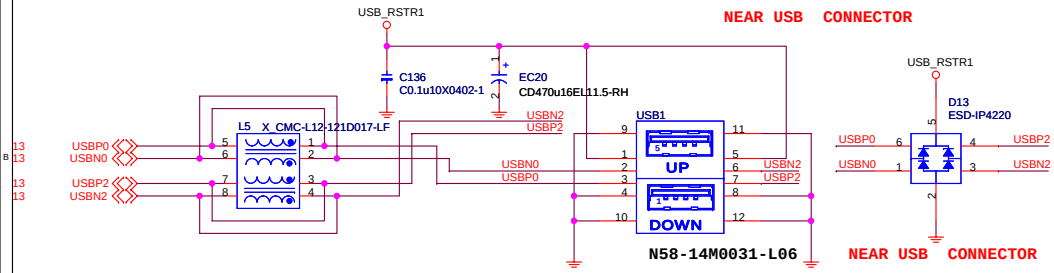
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



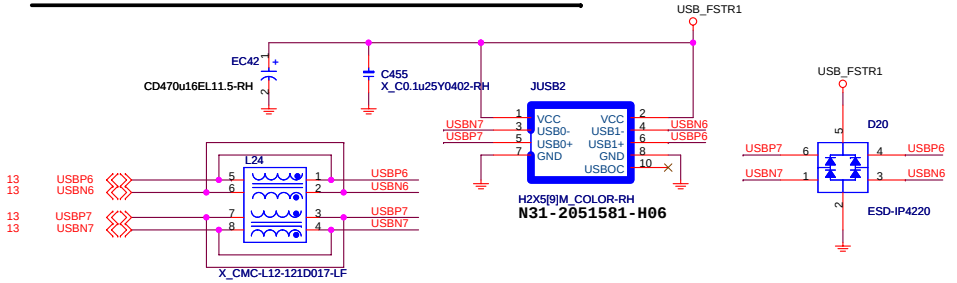
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



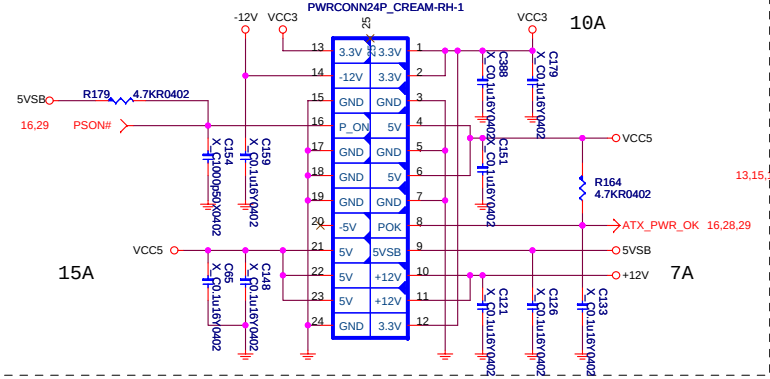
MICRO-STAR INT'L CO.,LTD

MS-7592

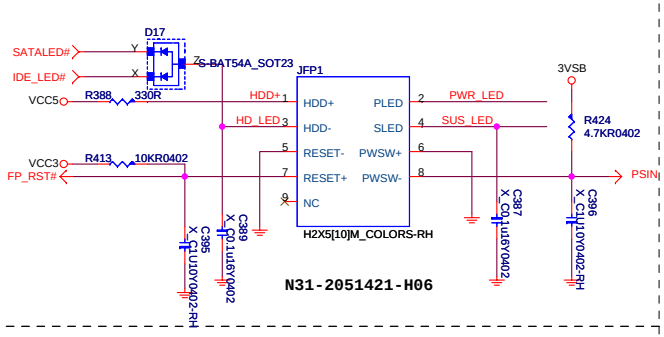
Size	Document Description	Rev
Custom	USB CONNECTORS	1.1

Date: Monday, December 15, 2008 | Sheet 25 of 33

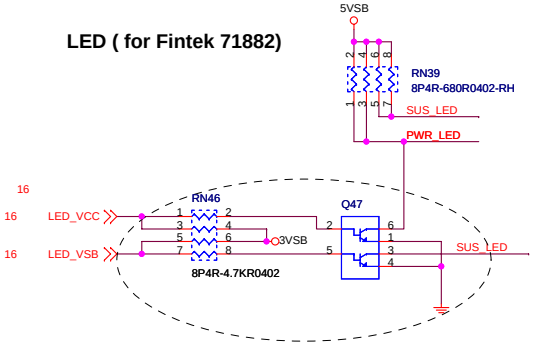
ATX Connector



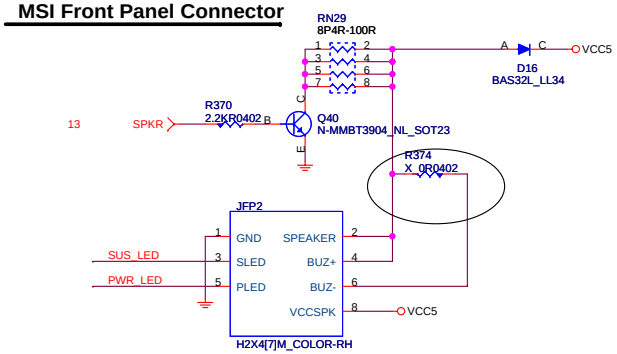
INTEL/PB Front Panel Connector



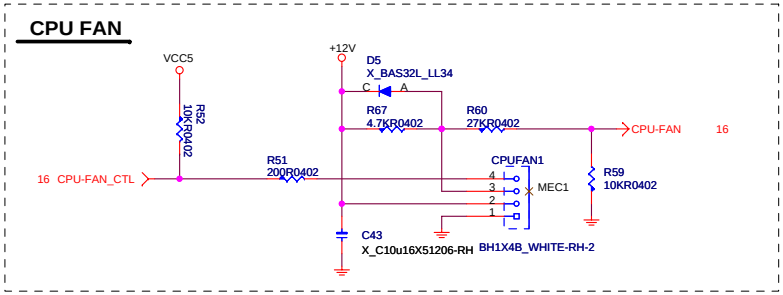
LED (for Fintek 71882)



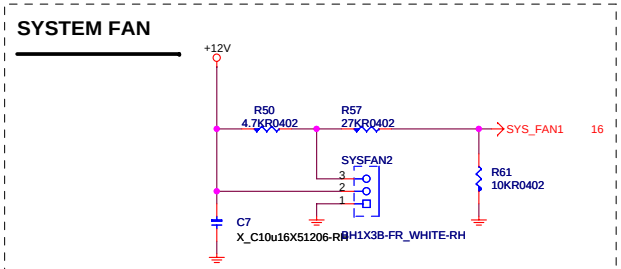
MSI Front Panel Connector



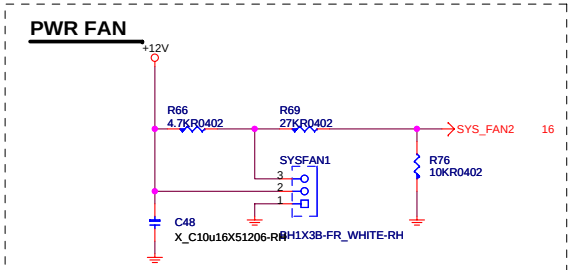
CPU FAN



SYSTEM FAN



PWR FAN



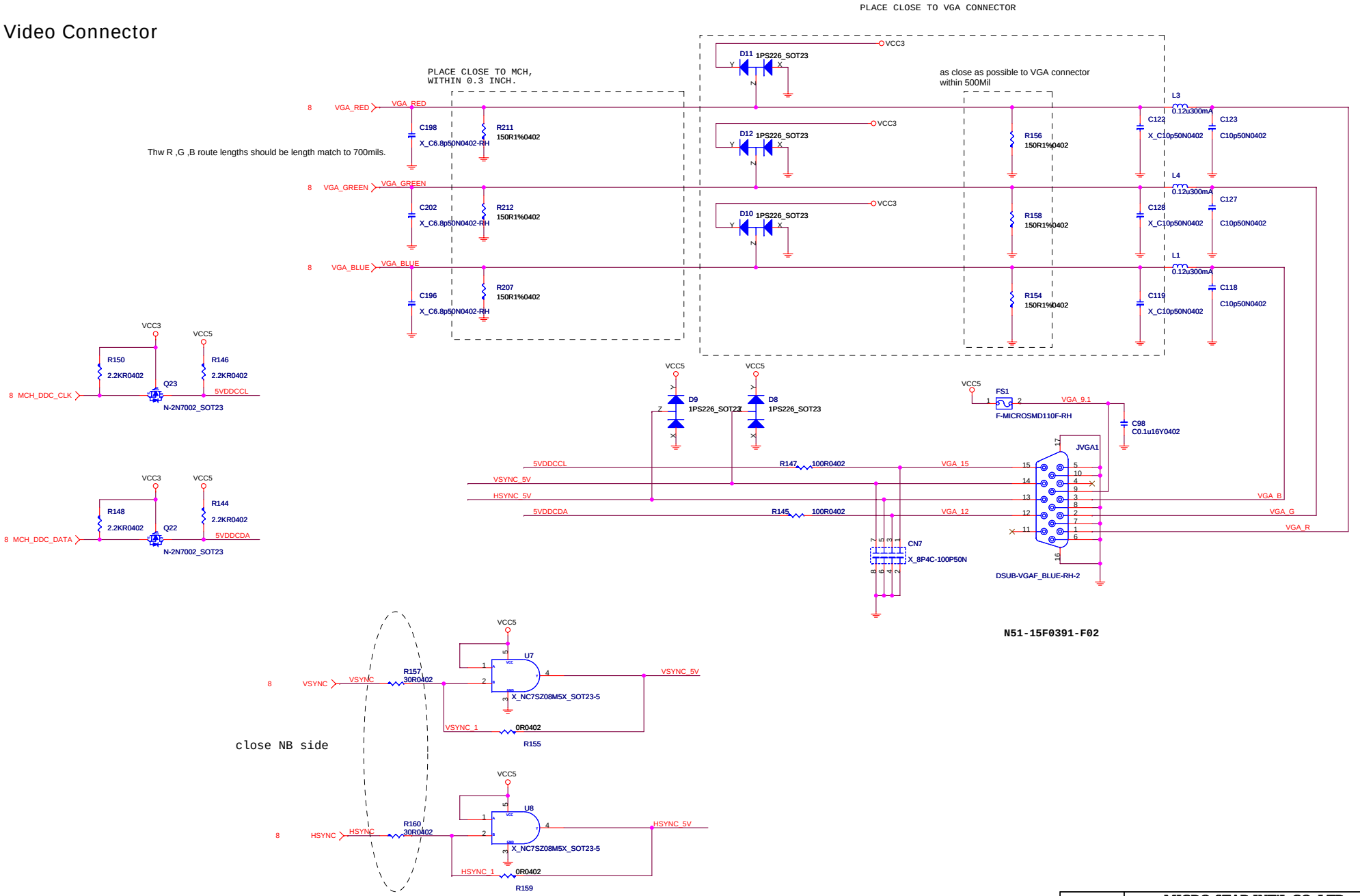
MICRO-STAR INT'L CO.,LTD

MS-7592

Size	Document Description	Rev
Custom	ATX & Front Panel & FAN	1.1

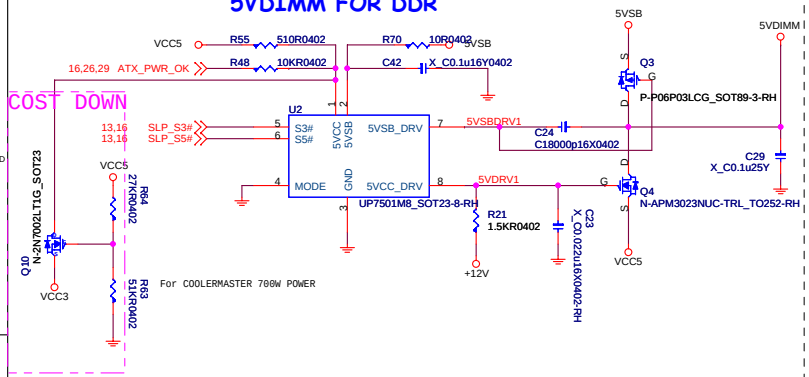
Date: Monday, December 15, 2008 Sheet 26 of 33

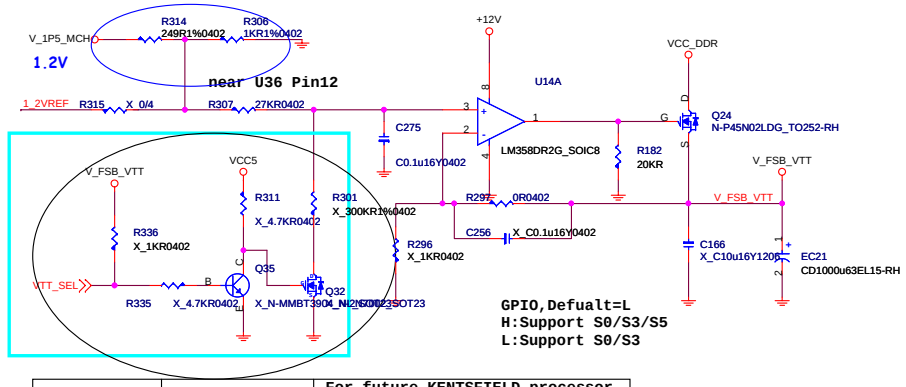
Video Connector



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7592	
Size: Custom	Document Description: VGA Connector	Rev: 1.1
Date: Monday, December 15, 2008	Sheet 27 of 33	

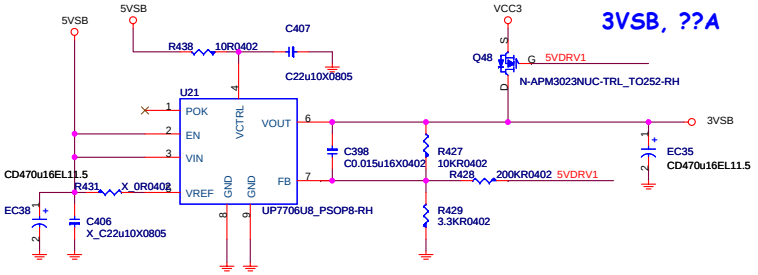
5VDIMM FOR DDR



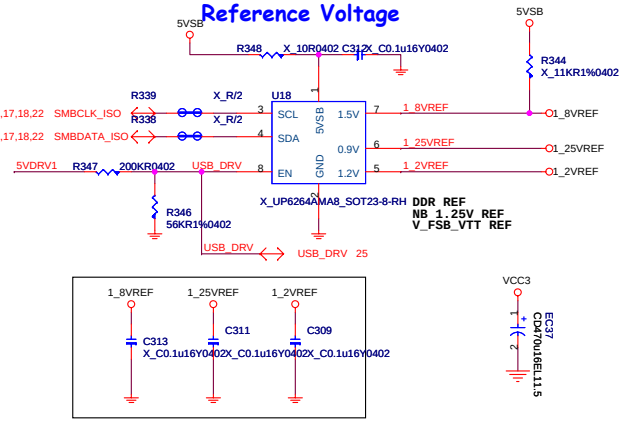


VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

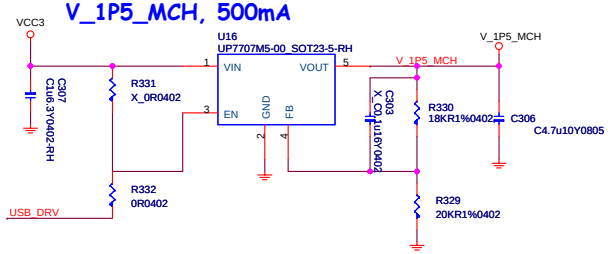
3VSB, ??A



Reference Voltage

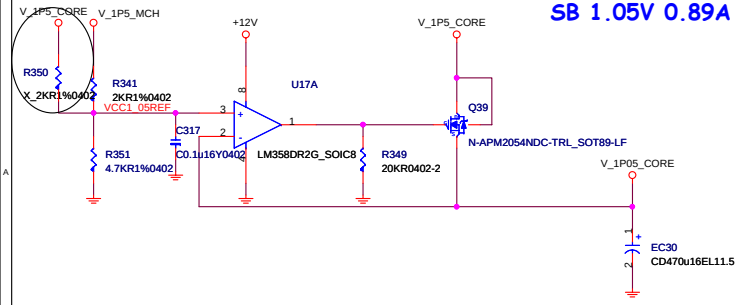


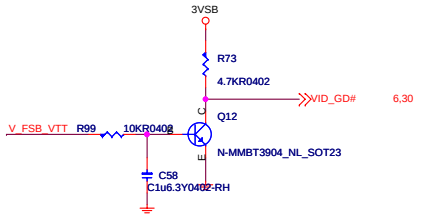
V_1P5_MCH, 500mA

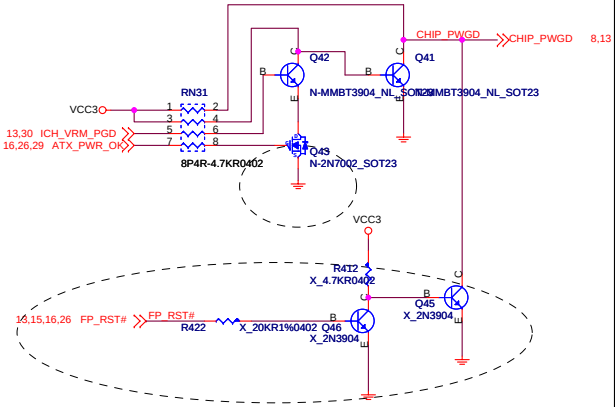


cost down u7707 UPI

SB 1.05V 0.89A

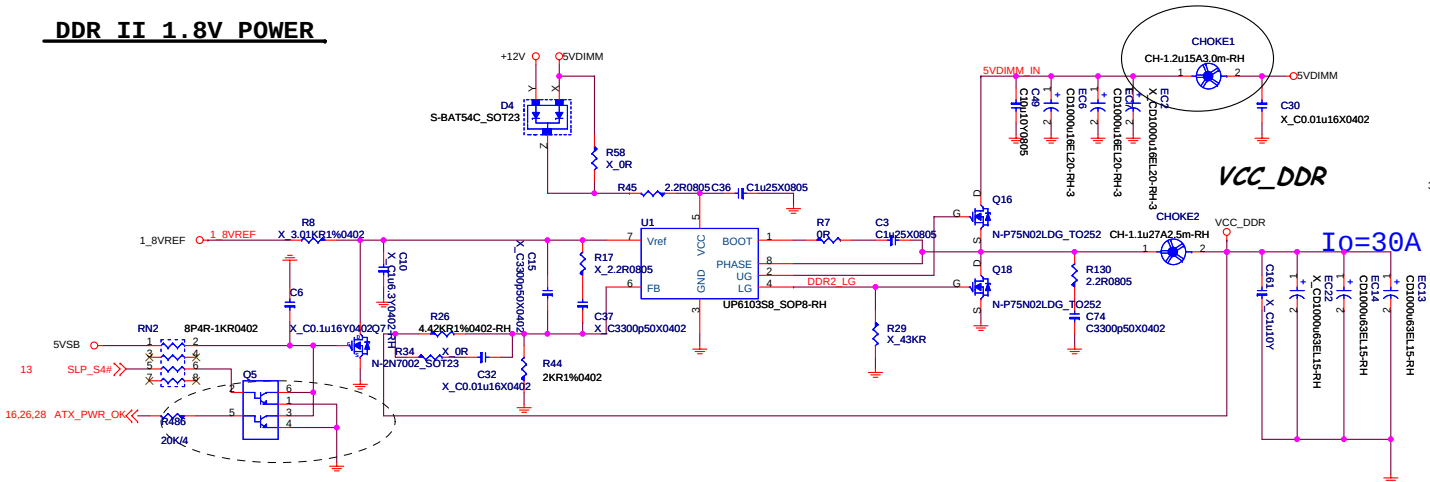






MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7592	
Size: Custom	Document Description: ACPI controller UPI	Rev: 1.1
Date: Monday, December 15, 2008	Sheet 28 of 33	

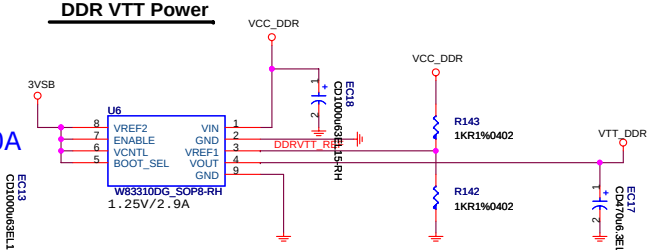
DDR II 1.8V POWER

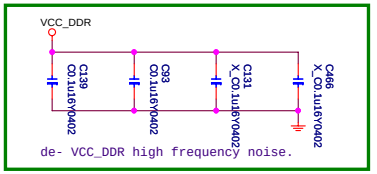


IF stuff UPI6264: use pin7 (Vref is 1.5V), pin 6 is 3.01K &15K ohm

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

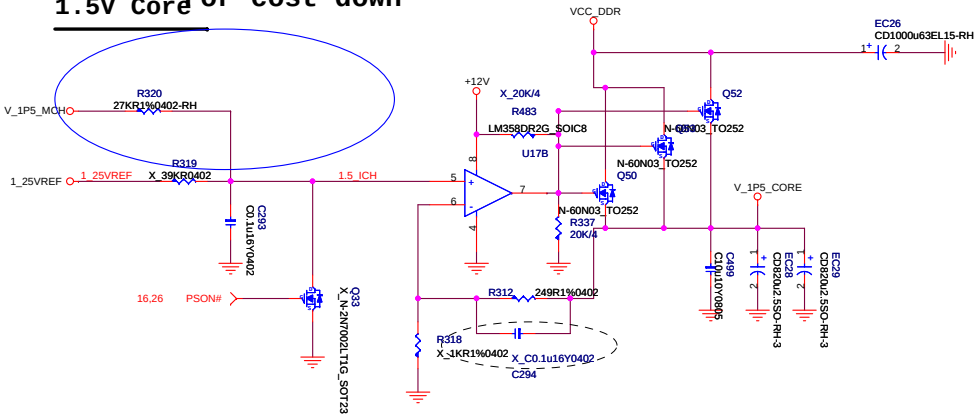
DDR VTT Power





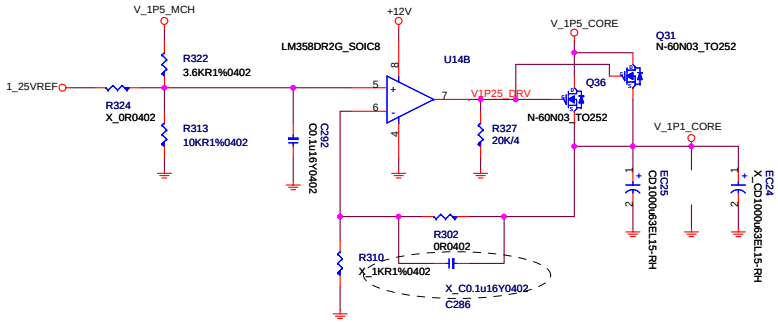
Do it need so many?

1.5V Core For cost down



? value=> 1.1V 1.5V=> 1.1V 3.6K /10K

V_1P1_CORE 18.1A+2.47A+2.94A



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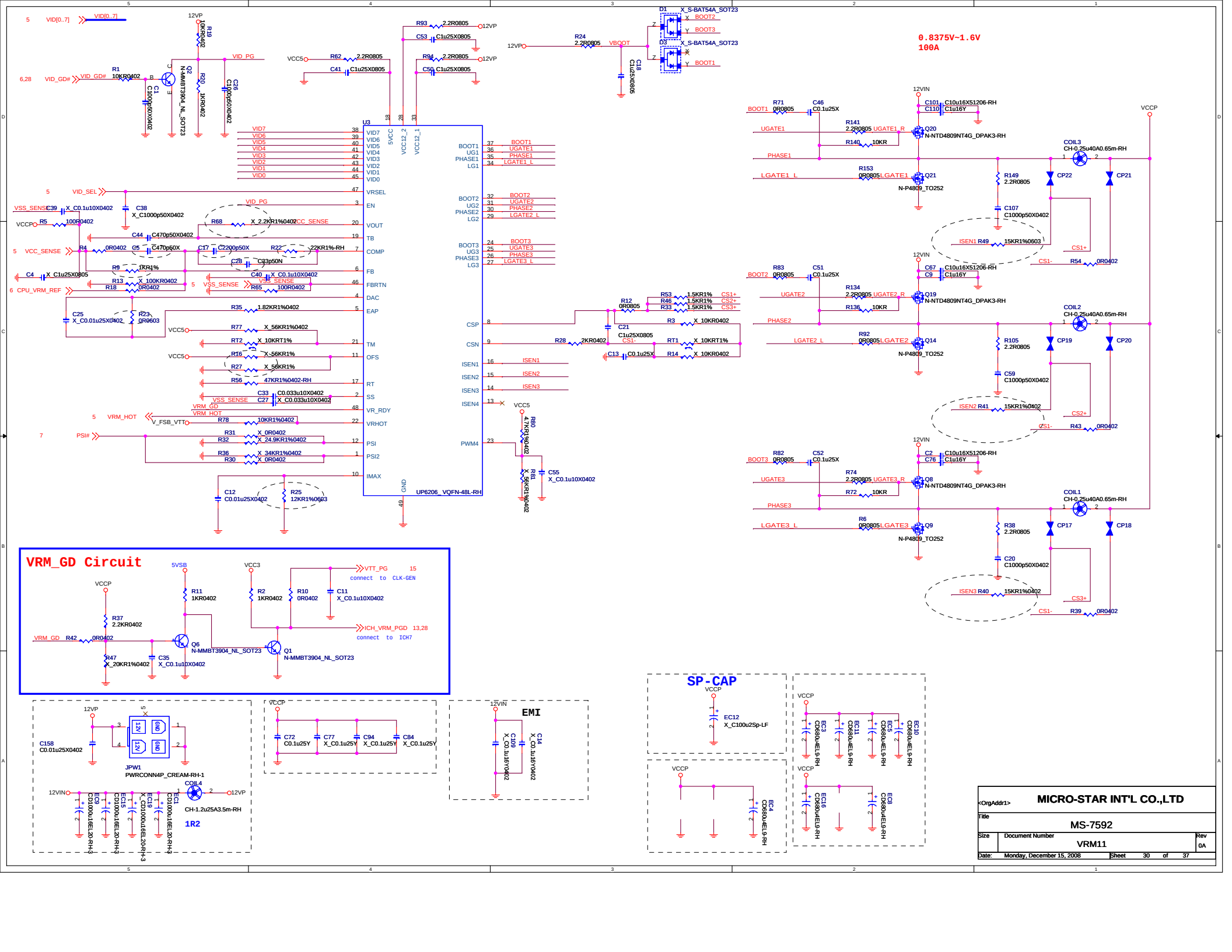
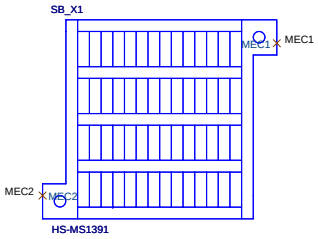
MS-7592

Size	Document Description	Rev
Custom	NB Core Power & DDR Power	1.1

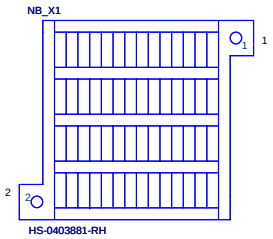
Date: Monday, December 15, 2008 Sheet 29 of 33


0.8375V~1.6V
100A
U3
UP6206_VQFN-48L-RH
VRM_GD Circuit
SP-CAP
EMI
JPW1
PWRCONN4P_CREAM-RH-1
COIL4
CH-1.2u25A3.5m-RH
1R2
COIL3
CH-0.25u40A0.65m-RH
COIL2
CH-0.25u40A0.65m-RH
COIL1
CH-0.25u40A0.65m-RH
MICRO-STAR INT'L CO.,LTD
MS-7592
VRM11

ICH7 HEATSINK

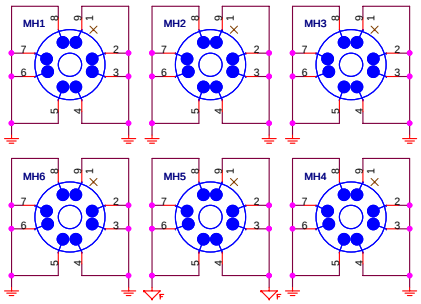


MCH HEATSINK

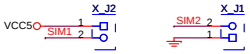


P80-075920A-E48
P80-075920A-G37

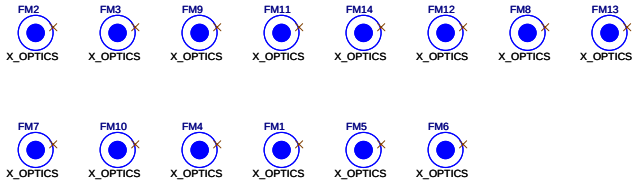
Mounting Holes



Simulation



Optics Orientation Holes



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MS-7592		
Size: Custom	Document Description: MANUAL PARTS	Rev: 1.1
Date: Monday, December 15, 2008	Sheet 31 of 33	

ICH7

GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPI0(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OOD12t	
GPIO6	SLOTOCC#	55	GPO	I/OOD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OOD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OOD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OOD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OOD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OOD12t	

PCI Config.

DEVICE	MCP1 INT PIN	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADRRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JCI1	*Chassis Intrusion*
Open	Normal
(1-2)	Chassis Open

JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

Title: BIOS Request Form
Size: C | Document Number: MS-7592 | Rev: 1.1
Date: Monday, December 15, 2008 | Sheet 32 of 33

0A Change list:

1. Add DMI Audio net name
2. Change LED Power pull high to 680 Change r20 to 1.5K
3. Change D10 D11 Power pull VCC5, Q20 Pull up VCC3
4. Delet R252 R254 C132 R22 C60,change U5 to I95-7523212-T07
5. Modify footprint : C_P3_5_D8_H9 NC_0402_6 NC_0603_10 C0805MSB C0603MS_BOT
6. Swap RN65 RN61 RN23 RN64 RN63 RN24 RN28 RN25 RN66 ; Delet EC20,
7. Add 5VCC TO 3VCC sequence
8. change TESTPIN30 to TPC20B
9. RENAME ,Swap RN37, X_J1 Change to GND , Change C300 C301 to 0.22UF
10. Modify V_1P25_CORE to G31

1.0 Change list:

1. U11 EN(pin3)change to USB_DRV
2. Add SIO pin55 SKTOCC# pull up to 3vsb
3. Swap RN26
4. add Control UP7501 power seqence

7592 Change list:

1. modify G31 to G41; LAN=> TRL8111DL; ALC888 - > change to ALC888S VC2;
SIO: I/O Fintek 882 - > Change to 889;
LAN : 8111C /8101E > Change to 8111DL / 8101E ;
Vcore ST6703   > Change to UPI 6206   2008/10/13

2.reserved 0 ohm to GND for ALC888s pin4
change DDR to quar choke (ckhoke1/2) 10/15
change Q27 to N7002 from 3904, change 2pcs N3904 to Q36 ;
chage LAN circuit => modify EL cap to MLCC for +3VSB; add 2n3904 for link100/1000 ;10/16
install copper to instand LXX :10/17

3. modify TPM footprint;=JLPC1_TPM 10/20
4. remove H/VSYNC to GND resistor, (only onboard VGA) 10/21
5:Pin 23 is GPO pin for8111DL. It is used forDSM function. 10/22
6. reserved SIO PECI_REQ# to ICH7 BMbusy# 10/23
7. reserved ITPM die to resistor (G41 no support ITPM 10/23
8, delect零件子阶(零件子堵) 10/24
9 ,reserved PSI function circuit, reserved PGNT#3 to Vcc3 for ICH Top Block-swap issue
reserved LPC_DRQ#0 pull high resistor (ICH7 &SIO interpull high) 10/24
10. H_VCCPLL 与VCCDQ_CRT分开以免layout时被相互干扰 10/24
11.H_COMP4 reserved Pul up R(DEMO board reserved); ICH7 pinAF24/AH25 for desttop is test pint,
for mobile is DPRSTP#/DPSLP#=> 0 ohm R to ICH7 no stuff , stuff CPU side pull high R to VTT; 10/26
12. PCIE slot footprint chage to SLOT_PCIEXP164_2(耳扣向上往CPU方向)
Clock part: cange 2 pcs 3904 to 1 2n3904 for layout size;10/27
13. reserved a DDR DIMM input EL cap ;
change VRM part some RC to 0603 footprint, reserved a SP_cap10/28
14. remove some NB TXX(test pad) for layout , 10/30
15: reserved RNXX for HDMI (RNXX intershort) P8; del TPM CONN TPMCLK 10P EMI cap; SWap RN64 .6&8 (CPUSEL2) 10/31
16: Swap RN15.1&3 , update NB_sink/EC36/37/R380 tol CIS library 11/03
17, modify some 0805 to 0603 cap for layout and reserved 1.1_core cap for cost (p8) ; change H/VSYNC_1 location for cost; 11/04
18: update NB ci library; change Audio 100uf cap to EL cap 11/05
19: modify test point footprint from tcp20B to testpin25
change VRM CS1/2/3+ to 1.5K ohm, reserved C8; 11/06
20 PLTRST_BU1# pull high from 220 ohm to 1K (VCC3) ==test signal 11/07
21: reservec SATALED# & AC_RST# pull high resistor 11/08
22 Footprint update： OSCC_MS 为 N_OSCC_MS 11/10
add rubber 6010: P/N:E25-7530010-C81 11/12
23 R40/R41 change 0402 value 11/21

7592 1.0 Change list:

1. SIO Version:B change to Version: C; SIO pin99(VCC) modify to 3VSB, pwok(pin80) modify to 3VSB ;
DMI CAP change to 0510 for SMT process ; update LAN_usb footprint, R181 for 8111DL, 8103E no install;1202
2> modify NB core and NB_sink P/N ;c211 chage to 0603;C359 chage to 3vsb for SIO Pin99 from Vcc3;
R158 R160 place NB side for SI bug,; add R486 for intel seq; 1212

Title: History		
Size: Custom	Document Number: MS-7592	Rev: 1.1
Date: Monday, December 15, 2008	Sheet 33 of 33	