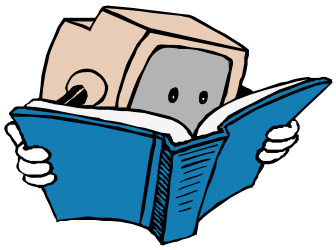
HITACHI

No. 0236

L37V01E
L37V01EA
L37V01U
L37VR1U
L37V01UA
L37VP01E
L37VP01U
L42VP01C
L42VP01S
L42VP01U
L42VP01UA



SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:

Before servicing this chassis, it is important that the service technician read the Safety Precautions and Product Safety Notices in this service manual.

ATTENTION:

Avant d'effectuer l'entretien du châssis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise“ und „Hinweise zur Produktsicherheit“ in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d'entretien peuvent faire l'objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

Contents

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

Colour Television

October 2007

1. INTRODUCTION

Analog front end consist of a main tuner, a pip tuner and IF decoders. The PLL tuners supply the IF signals and SAW filters are used for filtering and impedance matching between demodulator ICs and tuners. The main IF signal is demodulated by demodulator (DRX3961A) and the pip IF signal is demodulated by (TDA9885T). At the outputs of the demodulators, CVBS and QSS signals are obtained.

The main tuner CVBS, pip tuner CVBS, FAV CVBS, Scart1 CVBS, SVHS_Y, Scart2 CVBS/Y, DMP CVBS, IDTV/Scart3 CVBS/Y signals are applied to the video matrix switch (TEA6415). The outputs of the switch are main CVBS to video processor; pip CVBS to video decoder, scart1_out CVBS to scart1, scart2_out CVBS to scart2, scart3_out CVBS to scart3.

The video decoder IC (VPC3230) decodes to CVBS signal for the pip picture. The source for the pip picture can be CVBS from the video matrix switch, SVHS, Scart1, Scart2, Scart3 and DMP. The output of the decoder is 8 bits ITU601_PIP signal connected to video processor IC SVP LX66.

SVP-LX66 can support up to 1920x1080p panel. It consists of OSD, teletext, scaler, deinterlacer, 8/10-bit dual LVDS transmitter and HDMI blocks. The inputs to SVP LX66 are Scart2 RGB/DMP RGB, SC2/SC3 Chroma/SVHS Chroma, Scart1 RGB, main CVBS from video matrix switch, YPbPr, ITU601_PIP, HDMI, ITU601_IDTV, PC RGB. The output is the 8-bit LVDS signal to the panel.The SVP LX66 uses a DDR RAM (EM6A9320) for faster processing.

The main controller IC is M16C-M30620SPGP. The I/O assignments are as follows:

	NAME	TYPE	DESCRIPTION	Port	Pin
HDMI RELATED					
1	HDMI_HPLG	OUT	HotPlug output for HDMI-1 source device	P1.4	76
2	HDMI_HPLG2	OUT	HotPlug output for HDMI-2 source device	P8.0	22
3	HDMI_CEC	IN (*)	CEC input from HDMI cable	P1.5	75
4	HDMI_DTC	IN	HDMI detection for first input	P8.6	11
5	HDMI_DTC2	IN	HDMI detection for second input	P8.7	10
6	HDMI_DDC_WP	OUT	HDMI NVM write protect control for service	P9.4	3
7	SCDT	IN (*)	Sync Change Detection for HDMI	P8.4	18
POWER / PANEL RELATED					
8	PROTECT	IN	Indicates the power supply status	P1.7	73
9	STBY / CPU_GO	OUT	Controls the power supply on or off	P1.3	77
10	BLIGHT / PDP_GO	OUT	Controls the backlight	P1.2	78
11	DISP_EN	OUT	Controls the display enable or disable	P1.1	79
12	BLIGHT_LVL	PWM OUT	Controls the backlight level	P7.6	24
13	PANEL_VCC	OUT	Controls the power supply of the panel	P1.0	80
SERIAL DATA COMMUNICATION					
14	SDA	IN/OUT	I2C serial data line	P7.2	28
15	SCL	OUT	I2C clock line	P7.3	27
16	E2_SDA	IN/OUT	I2C serial data line for E2PROM	P10.7	89
17	E2_SCL	OUT	I2C clock line for E2PROM	P10.6	90
18	E2_WP	OUT	Controls the write protection of the E2PROM	P10.5	91
EXTENTION MODULES RELATED					
19	IDTV_RX	IN	IDTV UART receive	P6.2	36
20	IDTV_TX	OUT	IDTV UART transmit	P6.3	35
21	IDTV_IRQ	OUT	IDTV status change notification	P6.1	37
22	TVLINK	IN (*) / OUT	TVLink interrupt input / data output	P1.6	74
23	DMP_CTRL	OUT	Controls DMP module	P6.0	38
VIDEO RELATED					
24	LX_RST	OUT	Resets the LX66 video processor	P8.1	21
25	LX_INT	IN (*)	Interrupt notification from LX66	P8.3	19
26	RGB_SW_1	OUT	RGB switch control 1	P9.2	5
27	RGB_SW_2	OUT	RGB switch control 2	P9.3	4
APPLICATION					
28	IR	IN (*)	Remote control interrupt input	P8.2	20
29	LED_1	OUT	LED control 1	P9.0	7
30	LED_2	OUT	LED control 2	P9.1	6
31	MUTE_AMP	OUT	Mutes the audio amplifier	P9.7	100
32	SC1_PIN8	ADC IN	Scart 1 pin8 input measurement	P10.1	95
33	SC2_PIN8	ADC IN	Scart 2 pin8 input measurement	P10.2	94

34	SC3_PIN8	ADC IN	Scart 3 pin8 input measurement	P10.3	93
35	KEYB	ADC IN	Keyboard input	P10.0	97
36	SWU_RX	IN	UART receive for software upgrade	P7.1	29
37	SWU_TX	OUT	UART transmit for software upgrade	P7.0	30
38	RY_BY	IN	Ready/Busy indication from external flash	P5.1	45
39	LG_1/IRQPDP	IN	Interrupt Request from Plasma Display	P7.4	26
41	CHROMA_SW	OUT	Chroma Switch for SVHS	P7.5	25
42	DRX_RST	OUT	DRX reset	P9.6	1
43	VGA_STBY	IN	PC VGA standby detection	P9.5	2
44	SERV_DTC	IN	Service socket detection	P7.7	23
45	AC_INFO	IN	Alternate Current Information	P8.5	18

Table 1: Microcontroller I/O Assignments

The PC Audio L/R, DMP Audio L/R, IDTV/SC3 Audio L/R, YPbPr Audio L/R, Scart2 Audio L/R signals are switched via audio switch TEA6420. The outputs of the switch are two L/R audio signals.

MSP4411K is used for audio processing and it covers the sound processing of all analog TV-standards worldwide, as well as the NICAM digital sound standard. Audio outputs are connected to SC1/2/3 connector, audio line out, headphone, Speaker, subwoofer and S/PDIF connectors. The inputs to the MSP441K are two audio signals from audio switch, FAV_Audio_L/R, SC1_Audio_L/R, QSS signals from main and pip tuners, Tuner2 mono signal and HDMI I2S signal.

The AD8190 is a DVI/HDMI switch featuring equalised TMDS inputs and pre-emphasised TMDS outputs, ideal for systems with long cable runs between sources and sinks of video data. A disable feature sets the outputs to a high impedance state, reducing the power dissipation.

The primary function of the AD8190 is to switch one of two HDMI single-link sources to one output. Each HDMI source consists of four differential high-speed channels and four general purpose control lines. The switched HDMI signal is sent to the video processor IC.

2. CONTROLLER

2.1. Microcontroller: Renesas M16C M30620SPGP

General Description:

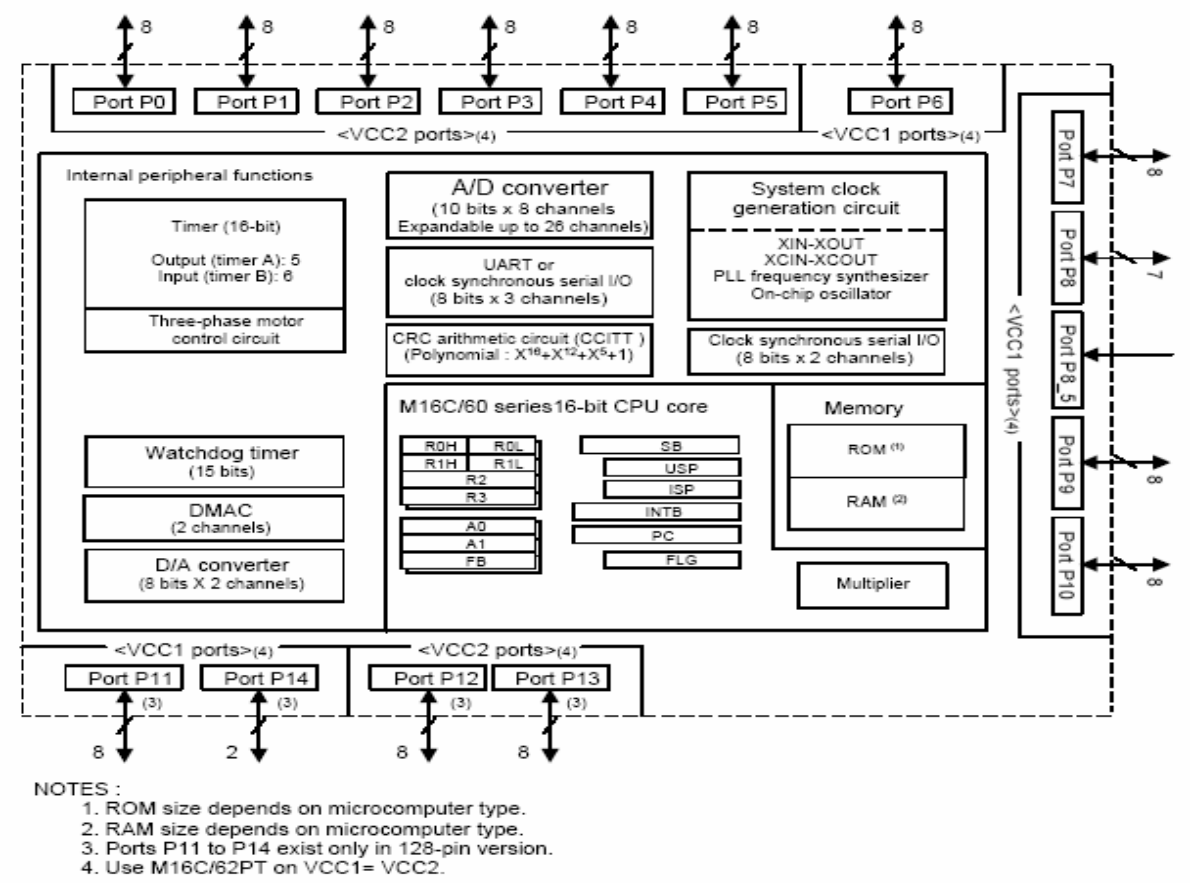
The M16C/62P Group (M16C/62P, M16C/62PT) of single-chip microcomputers are built using the high performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 80-pin, 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication and industrial equipment which requires highspeed arithmetic/logic operations.

General Features:

Main features of M16C are:

- 16-bit Multifunction Timer (Timer A and B): 11 channels
- UART/Clock Synchronous Serial Interface: 3 channels
- Clock Synchronous Serial Interface: 2 channels
- 10-bit A/D Converter: 26 channels
- 8-bit D/A Converter: 2 channels
- DMAC: 2 channels
- CRC Calculation Circuit
- Watchdog Timer
- Clock Generation Circuits: Main Clock Generation Circuit, Sub Clock Generation Circuit, On-chip Oscillator, PLL Synthesizer
- Oscillation Stop Detection Function
- Voltage Detection Circuit (Option) (Except for T Version and V Version)
- Interrupts: 29 internal factors, 8 external factors, 4 software factors
- Data Flash: 4KB (Flash Memory Version only)

Block Diagram:



NOTES :
1. ROM size depends on microcomputer type.
2. RAM size depends on microcomputer type.
3. Ports P11 to P14 exist only in 128-pin version.
4. Use M16C/62PT on VCC1= VCC2.

Figure 1: M16C Block Diagram

Pin Configuration:

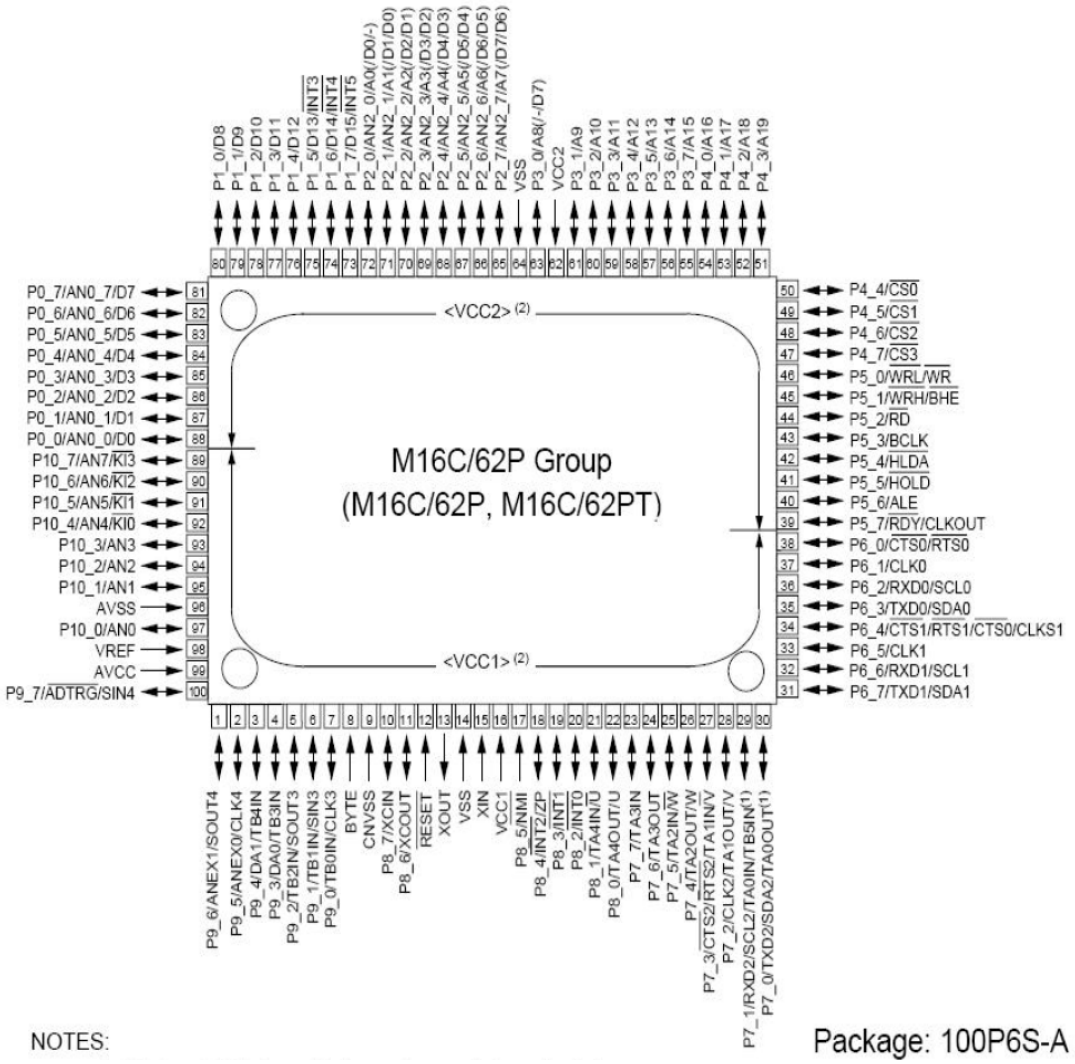


Figure 2: M16C Pin Configuration

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
1	99		P9_6			SOUT4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN		DA1	
4	2		P9_3		TB3IN		DA0	
5	3		P9_2		TB2IN	SOUT3		
6	4		P9_1		TB1IN	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$				
18	16		P8_4	$\overline{\text{INT2}}$	ZP			
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1		TA4IN/$\overline{\text{U}}$			
22	20		P8_0		TA4OUT/U			
23	21		P7_7		TA3IN			
24	22		P7_6		TA3OUT			
25	23		P7_5		TA2IN/$\overline{\text{W}}$			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2		
30	28		P7_0		TA0OUT	TXD2/SDA2		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0			$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
39	37		P5_7					$\overline{\text{RDY}}$/CLKOUT
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLAD}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
46	44		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
47	45		P4_7					$\overline{\text{CS3}}$
48	46		P4_6					$\overline{\text{CS2}}$
49	47		P4_5					$\overline{\text{CS1}}$
50	48		P4_4					$\overline{\text{CS0}}$

Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
FP	GP							
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8(/-/D7)
64	62	VSS						
65	63		P2_7				AN2_7	A7(/D7/D6)
66	64		P2_6				AN2_6	A6(/D6/D5)
67	65		P2_5				AN2_5	A5(/D5/D4)
68	66		P2_4				AN2_4	A4(/D4/D3)
69	67		P2_3				AN2_3	A3(/D3/D2)
70	68		P2_2				AN2_2	A2(/D2/D1)
71	69		P2_1				AN2_1	A1(/D1/D0)
72	70		P2_0				AN2_0	A0(/D0/-)
73	71		P1_7	$\overline{\text{INT5}}$				D15
74	72		P1_6	$\overline{\text{INT4}}$				D14
75	73		P1_5	$\overline{\text{INT3}}$				D13
76	74		P1_4					D12
77	75		P1_3					D11
78	76		P1_2					D10
79	77		P1_1					D9
80	78		P1_0					D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	$\overline{\text{KI3}}$			AN7	
90	88		P10_6	$\overline{\text{KI2}}$			AN6	
91	89		P10_5	$\overline{\text{KI1}}$			AN5	
92	90		P10_4	$\overline{\text{KI0}}$			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7			SIN4	$\overline{\text{ADTRG}}$	

Table 2: M16C Pin Descriptions

2.2. Flash IC SST39VF088

General Description:

The SST39VF088 device is a 1M x8 CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF088 writes (Program or Erase) with a 2.7-3.6V power supply. It conforms to JEDEC standard
pinouts for x8 memories. Featuring high performance Byte-Program, the SST39VF088 device provides a typical Byte-Program time of 14 µsec. The devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and
Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.The SST39VF088 device is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. They also improve flexibility while lowering the cost for program, data, and configuration storage applications.
The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles. To meet high density, surface mount requirements, the SST39VF088 is offered in 48-lead TSOP packaging. See below figure for pin assignments.

General Features:

• Organised as 1M x8
• Single Voltage Read and Write Operations
– 2.7-3.6V
• Superior Reliability
– Endurance: 100,000 Cycles (typical)
– Greater than 100 years Data Retention
• Low Power Consumption (typical values at 5 MHz)
– Active Current: 12 mA (typical)
– Standby Current: 4 µA (typical)
• Sector-Erase Capability
– Uniform 4 kByte sectors
• Block-Erase Capability

– Uniform 64 kByte blocks
• Fast Read Access Time:
– 70 and 90 ns
• Latched Address and Data
• Fast Erase and Byte-Program
– Sector-Erase Time: 18 ms (typical)
– Block-Erase Time: 18 ms (typical)
– Chip-Erase Time: 70 ms (typical)
– Byte-Program Time: 14 µs (typical)
– Chip Rewrite Time: 15 seconds (typical)
• Automatic Write Timing
– Internal VPP Generation
• End-of-Write Detection
– Toggle Bit
– Data# Polling
• CMOS I/O Compatibility
• JEDEC Standard
– Flash EEPROM Pinouts and command sets
• Packages Available
– 48-lead TSOP (12mm x 20mm)

Pin Configuration:

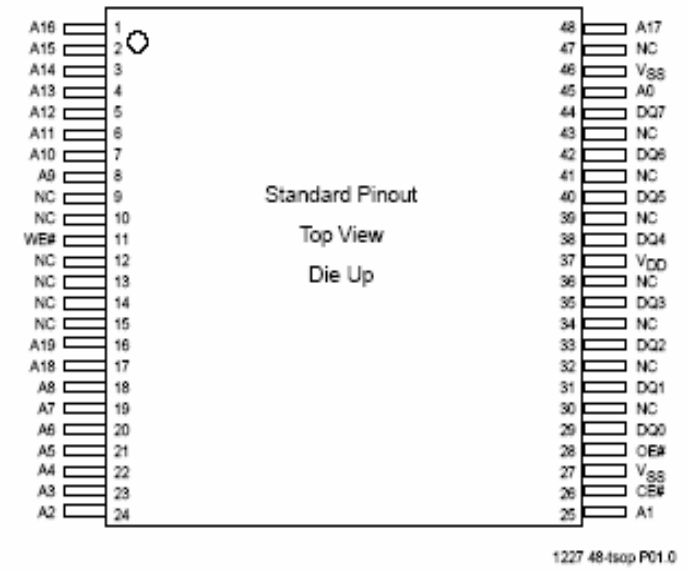


Figure 3: Flash IC Pin Configuration

Symbol	Pin Name	Functions
A_{MS}[1]-A_0	Address Inputs	To provide memory addresses. During Sector-Erase A_{MS}-A_{12} address lines will select the sector. During Block-Erase A_{MS}-A_{16} address lines will select the block.
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V for SST39VF088
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

T2.0 1227

1. A_{MS} = Most significant address
   A_{MS} = A_{19} for SST39VF088

Table 3: Flash IC Pin Descriptions

2.3. 32K I2C Serial EEPROM: 24LC32A

General Description:

The Microchip Technology Inc. 24AA32A/24LC32A (24XX32A*) is a 32-kbit Electrically Erasable PROM.The device is organised as four blocks of 8K x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1 uA and 1 mA, respectively. It has been developed for advanced, lowpower applications such as personal communications or data acquisition. The 24XX32A also has a page write capability for up to 32 bytes of data. Functional address lines allow up to eight devices on the same bus, for up to 256 kbits address space. The 24XX32A is available in the standard 8-pin PDIP, surface mount SOIC,
TSSOP and MSOP packages.

General Features:

• Single supply with operation down to 1.8V
• Low-power CMOS technology
- 1 mA active current typical
- 1uA standby current (max.) (I-temp)
• Organised as 4 blocks of 8k bits (32k bit)
• 2-wire serial interface bus, I2C™ compatible
• Cascadable for up to eight devices
• Schmitt Trigger inputs for noise suppression
• Output slope control to eliminate ground bounce
• 100 kHz (<2.5V) and 400 kHz (≥2.5V)
compatibility
• Self-timed write cycle (including auto-erase)
• Page write buffer for up to 32 bytes
• 2 ms typical write cycle time for page write

• Hardware write-protect for entire memory
• Can be operated as a serial ROM
• Factory programming (QTP) available
• ESD protection > 4,000V
• 1,000,000 erase/write cycles
• Data retention > 200 years
• 8-lead PDIP, SOIC, TSSOP and MSOP packages
• Standard and Pb-free finishes available
• Available temperature ranges:
- Industrial (I): -40°C to +85°C
- Automotive (E): -40°C to +125°C

Block Diagram:

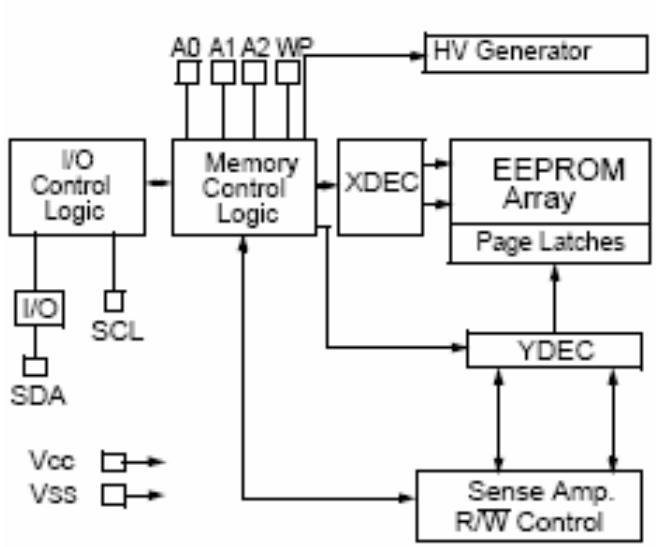


Figure 4: Serial EEPROM Block Diagram

Pin Configuration:

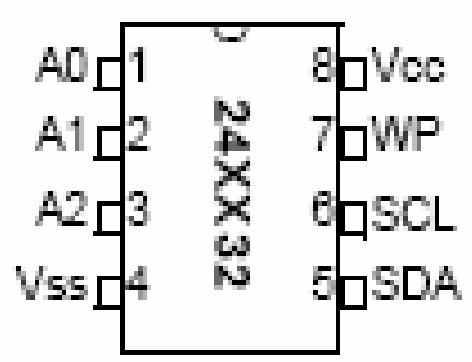


Figure 5: Serial EEPROM Pin Configuration

3. TUNING AND IF DECODING

3.1. Tuner

The tuners used in the design are combined VHF, UHF tuners suitable for CCIR systems B/G, H, L, L', I/I', and D/K. The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info on one of the tuners in use.

Description:

The UV1316MK4 tuner belongs to the UV1300 family of third generation WSP tuners, which are designed to meet a wide range of TV applications. It is a full band tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance is designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple.

Features:

Member of UV1300 MK4 family of small-sized UHF/VHF tuners

- Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
- Digitally-controlled (PLL) tuning via I2C-bus
- Fast 400kHz I2C bus protocol compatible with 3.3V and 5V micro controllers
- Off-air, S-cable and hyperband channels from 48.25 MHz to 863.25MHz inclusive
- World standardized mechanical dimensions and pinning. Horizontal mounting is optionally available
- Various connector types available
- EURO content available.

Pin Configuration:

Pin	Symbol	Description
1	AGC	Automatic Gain Control Voltage
2	TU	Tuning Voltage Monitor(Output)
3	AS	I2C Bus Address Select
4	SCL	I2C Bus Serial Clock
5	SDA	I2C Bus Serial Data
6	N.C.	Not Connected
7	Vs	Supply Voltage +5V
8	ADC	ADC Input
9	Vst	Fixed Tuning Supply Voltage +32V
10	I.F out 2 / d.n.c	Symmetrical I.F output 2 / Do not connect for asymmetrical
11	I.F out 1	Asymmetrical I.F Output / Symmetrical I.F output 1
M1,M2,M3,M4	GND	Mounting Tags (Ground)

Table 4: UV1316 MK4 Pin Descriptions

Block Diagram:

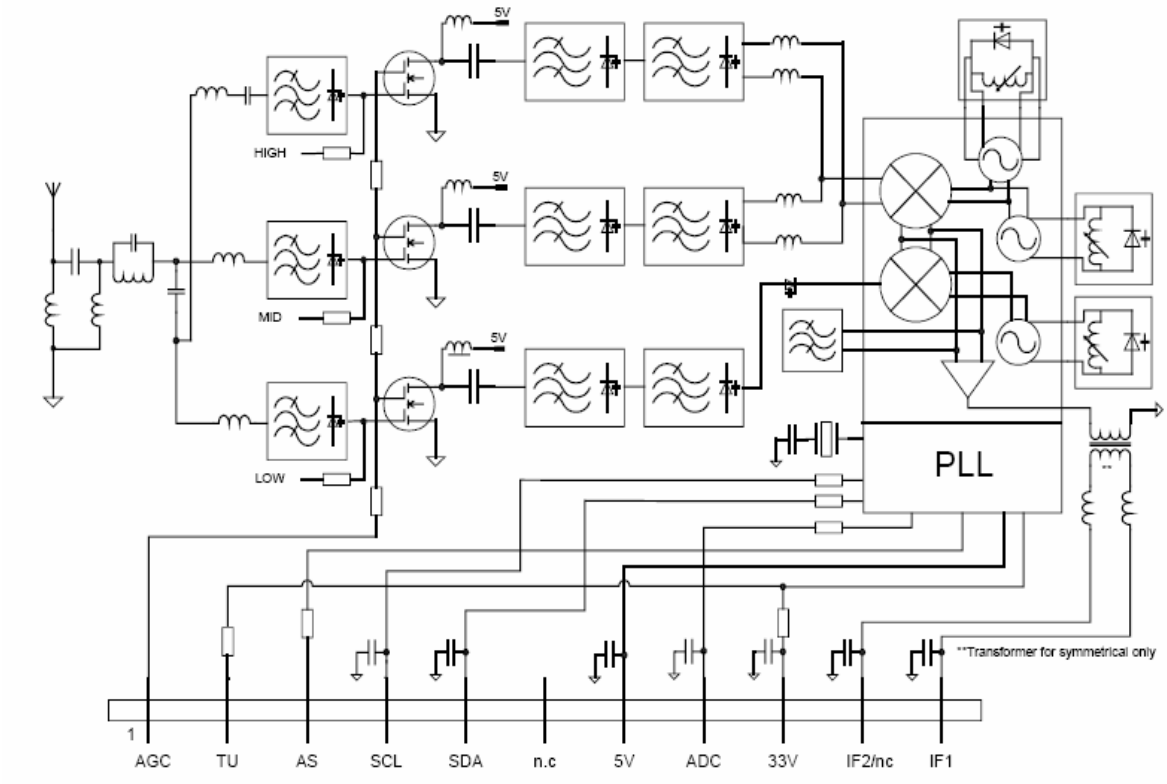


Figure 6: UV1316 MK4 Block Diagram

3.2. IF Demodulator: Micronas DRX3961A

DRX 3961A is used to extract CVBS and audio information from the IF output of the tuner.

Features:

- Multistandard QSS IF processing with a single SAW filter
- Programmable IF frequency between 30 and 60 MHz
- DSP-based IF processing for the following standards: B/G, D/K, I, L/L', and M/N
- Standard specific digital signal processing for channel filtering, audio/video splitting, group delay equalisation (programmable), video AGC and delayed tuner AGC
- Digital picture carrier recovery
- Automatically frequency-adjusted Nyquist slope over complete lock-in frequency range, which eliminates the need of fine tuning
- Fast AGC algorithms for tuner, video, and SIF outputs

- Programmable tuner take-over point (TOP)
- No sound traps required for video output
- FM radio capability without external components and with standard TV tuner
- I2C bus interface

Pin Configuration:

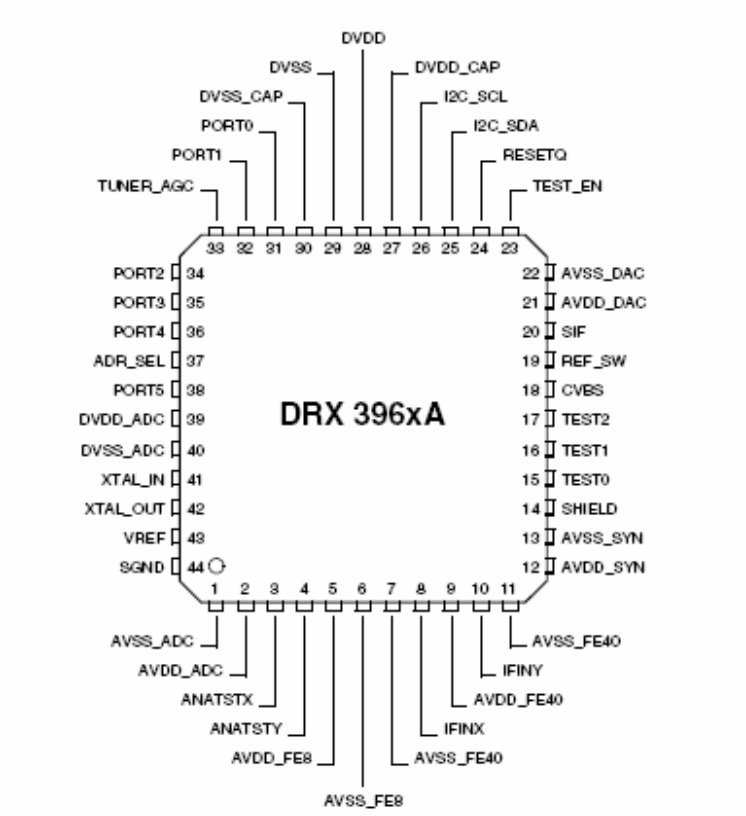


Figure 7: DRX 3961A Pin Configurations

Block Diagram:

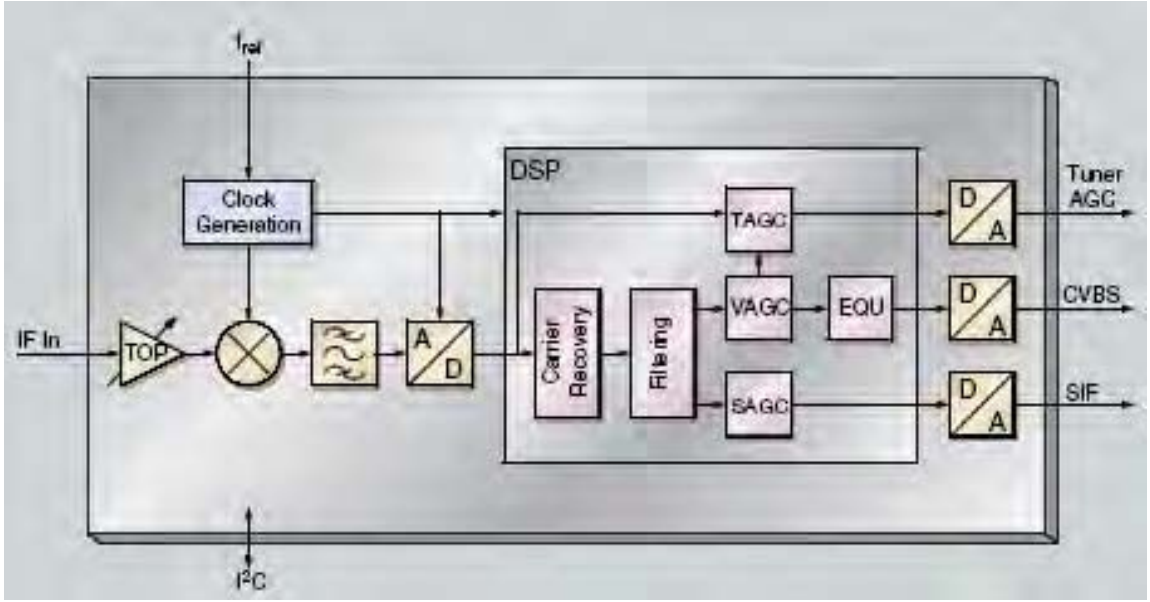


Figure 8: DRX 3961A Block Diagram

3.3. IF Demodulator:TDA9886T

Description:

The TDA9886T is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal PLL demodulator for negative modulation only and FM processing.
The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

Features:

· 5 V supply voltage
· Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier, AC-coupled
· Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
· Gated phase detector for L and L-accent standard
· Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I2C-bus
· Digital acquisition help, VIF frequencies of 33.4, 33.9,38.0, 38.9, 45.75, and 58.75 MHz
· 4 MHz reference frequency input: signal from Phase-Locked Loop (PLL) tuning system or operating as crystal oscillator
· VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
· External AGC setting via pin OP1
· Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I2C-bus

· TakeOver Point (TOP) adjustable via I2C-bus or alternatively with potentiometer
· Fully integrated sound carrier trap for 4.5, 5.5, 6.0, and 6.5 MHz, controlled by FM-PLL oscillator
· Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled
· SIF-AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I2C-bus
· AM demodulator without extra reference circuit
· Alignment-free selective FM-PLL demodulator with high linearity and low noise
· Four selectable I2C-bus addresses
· I2C-bus control for all functions
· I2C-bus transceiver with pin programmable Module Address(MAD)

Pin Configuration:

Symbol	Pin	Description
VIF1	1	VIF differential input 1
VIF2	2	VIF differential input 2
n.c.	-	not connected
OP1	3	output port 1; open-collector
FMPLL	4	FM-PLL for loop filter
DEEM	5	de-emphasis output for capacitor
AFD	6	AF decoupling input for capacitor
DGND	7	digital ground
n.c.	-	not connected
AUD	8	audio output
TOP	9	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	I2C-bus data input and output
SCL	11	I2C-bus clock input
SIOMAD	12	sound intercarrier output and MAD select with resistor
n.c.	-	not connected
n.c.	13	not connected
n.c.	-	not connected
TAGC	14	tuner AGC output
REF	15	4 MHz crystal or reference signal input
VAGC	16	VIF-AGC for capacitor
n.c.	-	not connected
CVBS	17	composite video output
n.c.	-	not connected
AGND	18	analog ground
VPLL	19	VIF-PLL for loop filter

VP	20	supply voltage
AFC	21	AFC output
OP2	22	output port 2; open-collector
n.c.	-	not connected
SIF1	23	SIF differential input 1 and MAD select with resistor
SIF2	24	SIF differential input 2 and MAD select with resistor
n.c.	-	not connected
n.c.	-	not connected

Table 5: TDA9886T Pin Descriptions

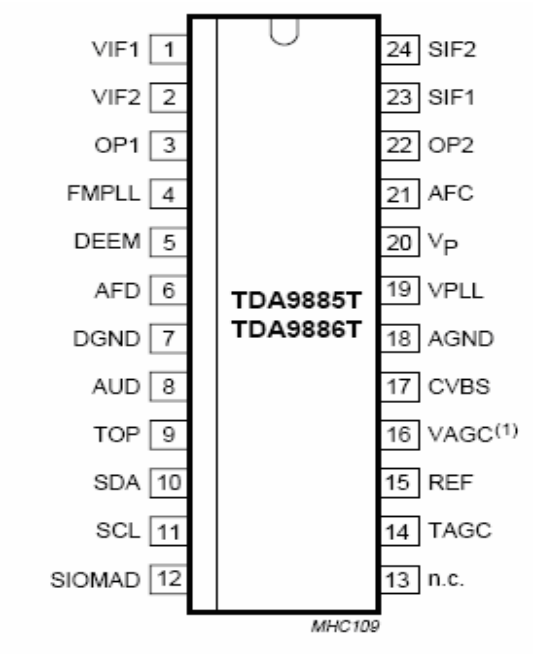


Figure 9: TDA9886T Pin Configurations

3.4. SAW (Surface Acoustic Wave) Filter: Epcos X6966M

X6966M is a bandpass IF filter at f_c = 36.125 MHz with tinned CuFe alloy terminals.

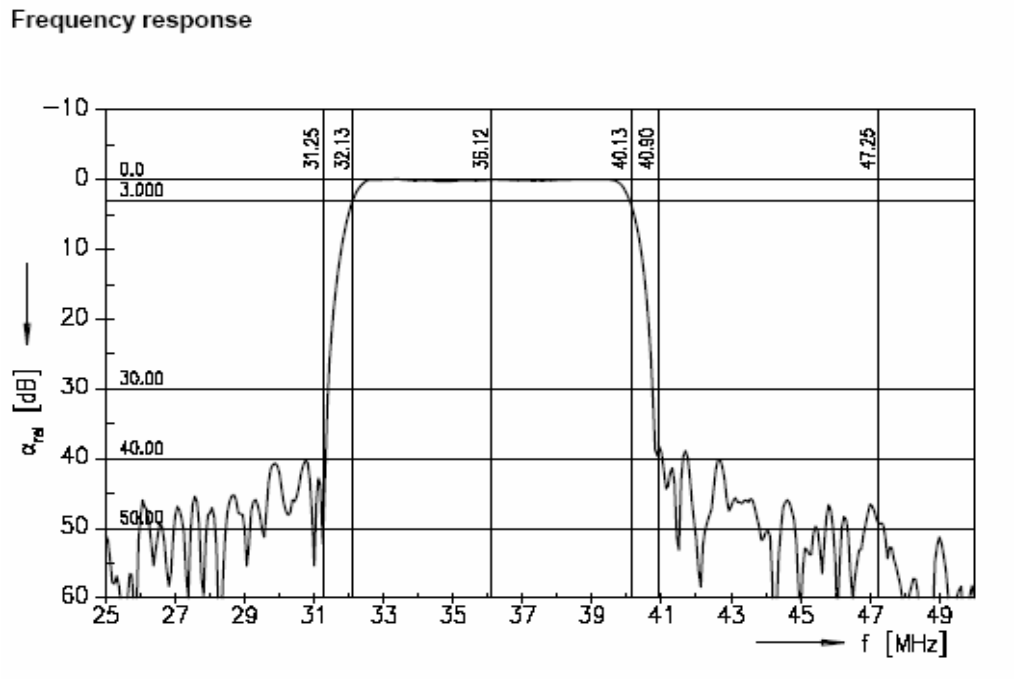


Figure 10: Frequency Response of X6966M

4. AUDIO PROCESSING

4.1. Sound Processor: Micronas MSP 4411K

Description:

MSP 4411K is a single-chip TV sound demodulator, decoder and baseband audio processor.

Features:

- Alignment-free decoding of all TV audio standards
- US BTSC audio with DBX noise reduction and SAP decoding
- Japanese EIA-J stereo
- Digital NICAM stereo
- All 2-carrier TV Audio standards
- (Very) High deviation modes HDEV2, 3
- Automatic Standard Detection (ASD)
- Automatic Sound Select (ASS) switches mono/stereo/bilingual without controller interaction
- Delay line for “Lip Sync”
- SRS TruSurround XT (optional)
- BBE High Definition Sound (optional)
- Virtual Dolby Surround
- Equaliser, Tone control, Subwoofer filter

- Micronas BASS, Micronas VOICE
- Two SIF inputs to the Demodulator
- 8-channel I^2S inputs with sampling rate converter
- Analog stereo line inputs (to A/D or switched to line outputs)
- Loudspeaker D/A for L, R, Sub channels with analog volume
- Headphone D/A with analog volume
- I^2S outputs
- S/PDIF output

Block Diagram:

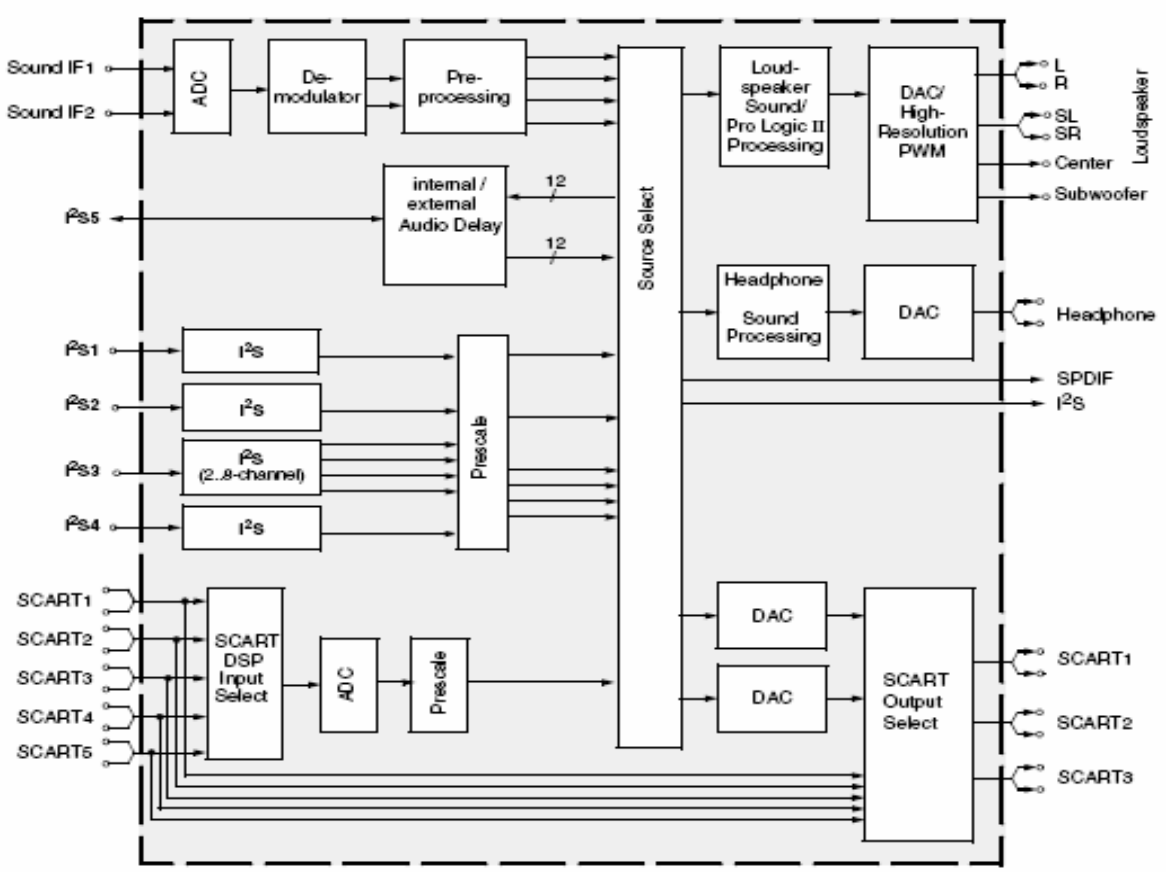


Figure 11: MSP44xyK / MSP46xyK

4.2. Audio Switch: ST TEA6420

Description:

The TEA6420 switches 5 stereo audio inputs on 4 stereo outputs. All the switching possibilities are changed through the I2C bus.

Features:

- 5 stereo inputs
- 4 stereo ouputs
- Gain Control (0/2/4/6dB/Mute) for each output
- Serial Bus Controlled
- Very low Noise
- Very low Distortion

Block Diagram:

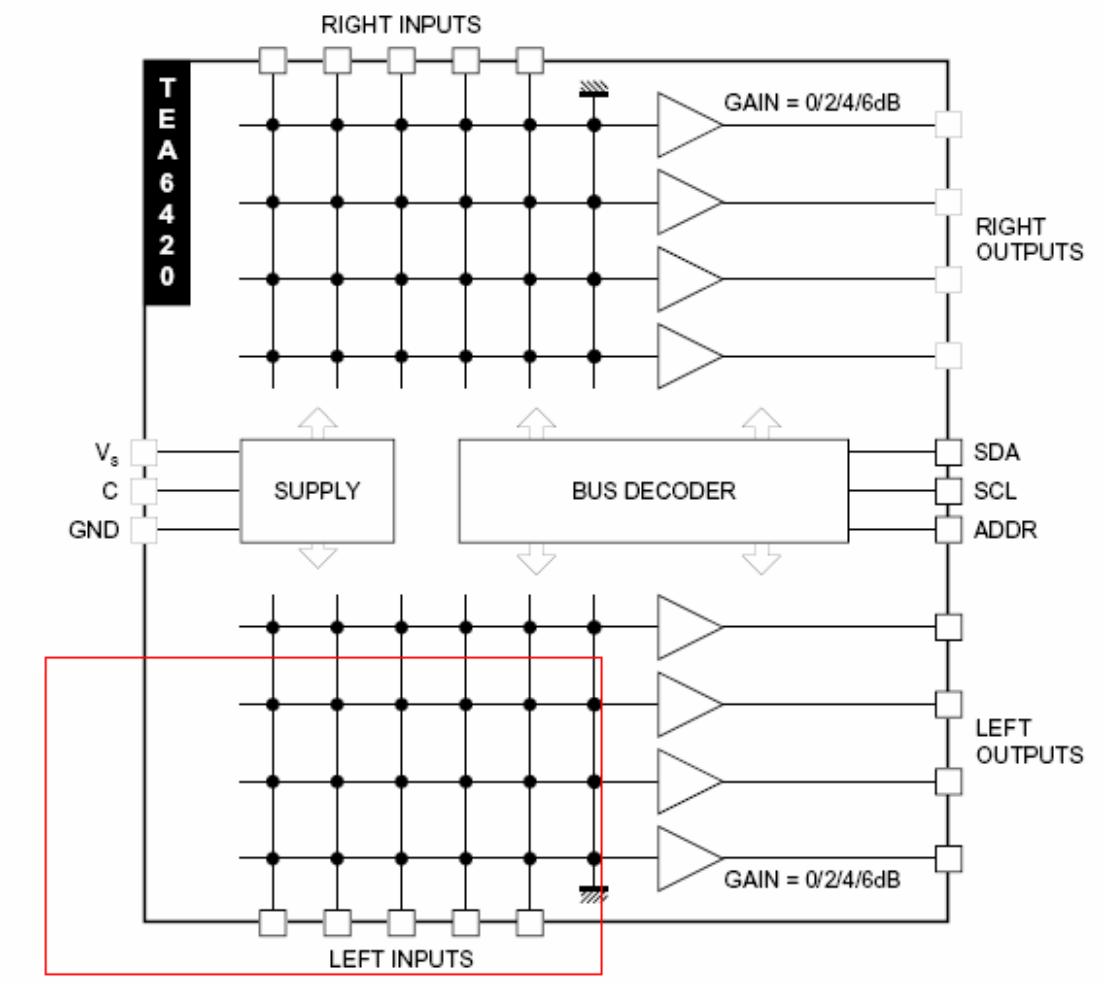


Figure 12: TEA6420 Block Diagram

Pin Connections:

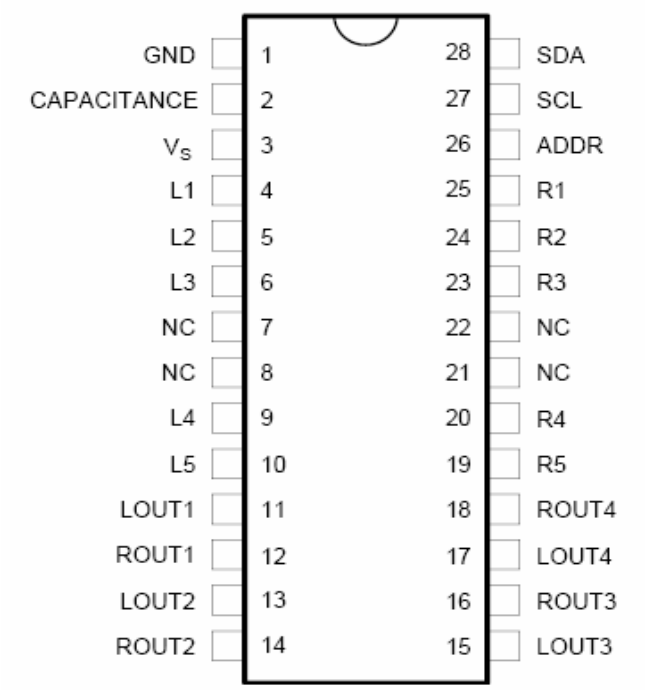


Figure 13: TEA 6420 Pin Configuration

4.3. Headphone Amplifier: Philips TDA1308

Description:

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

Features:

- Operating temperature range: -40 to +85 C
- No switch ON/OFF clicks
- Short-circuit resistant
- Signal-to-noise ratio: 110 dB
- Total harmonic distortion: 0.001 %

Block Diagram:

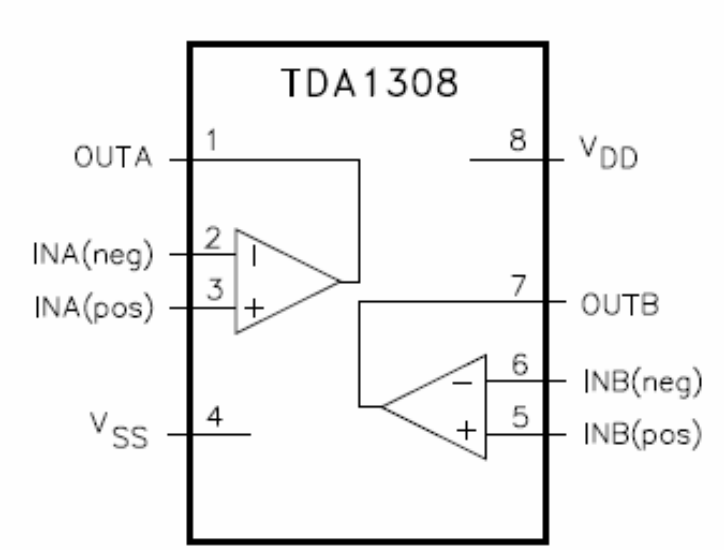


Figure 14: TDA1308 Block Diagram

Pin Configuration:

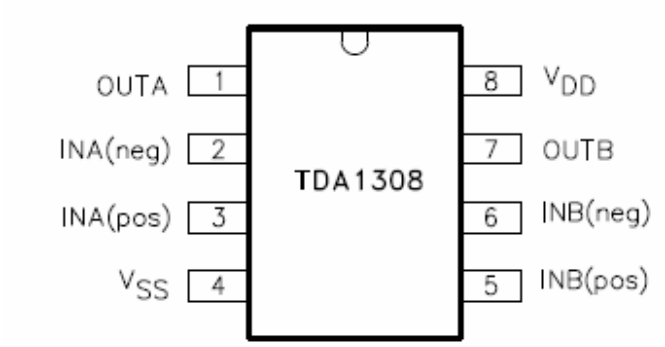


Figure 15: TDA1308 Pin Configuration

SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
V_{DD}	8	positive supply

Table 6: TDA1308 Pin Descriptions

5. VIDEO PROCESSING

5.1. Video Processor: TRIDENT SVP LX66

Description:

The SVPTMLX66 video processor is a highly integrated system-on-a-chip device, targeting the converging HDTV-ready and PC-ready LCD TV, PDP TV, and DLP TV applications where high precision processing of video and data are the requirements.
SVP LX66 has a total of four video input ports: one analog port, one HDMI port, and two digital ports: PortA and PortB. LVDS output is either dual or single pixel mode.

Features:

- Integrated HDMi Receiver with HDCP up to 135 MHz.
- Integrated 6th Generation Motion and Edge Adaptive De-interlacing
- Integrated ADC
- PC Auto Tune
- Built-in dual 8/10-bit LVDS Transmitter
- Vertical Keystone for Projector
- Advanced 6th generation cubic-4 image scaling engine.
- Horizontal and vertical mirror image inversion
- DNR-Digital Temporal and Spatial Noise Reduction Filter
- Advanced Chroma Processing
- Dynamic Contrast Function
- Green Colour Stretch, blue colour stretch, skin colour enhancement
- Integrated 6th Generation Motion Adaptive 3D Digital Comb Video Decoder with Programmable Filter
- Inverse Colour Space Conversion
- Trident Proprietary LCD-BRITETM Technology for LCD Overdrive
- Interlaced and Progressive Scan Refresh

Block diagram:

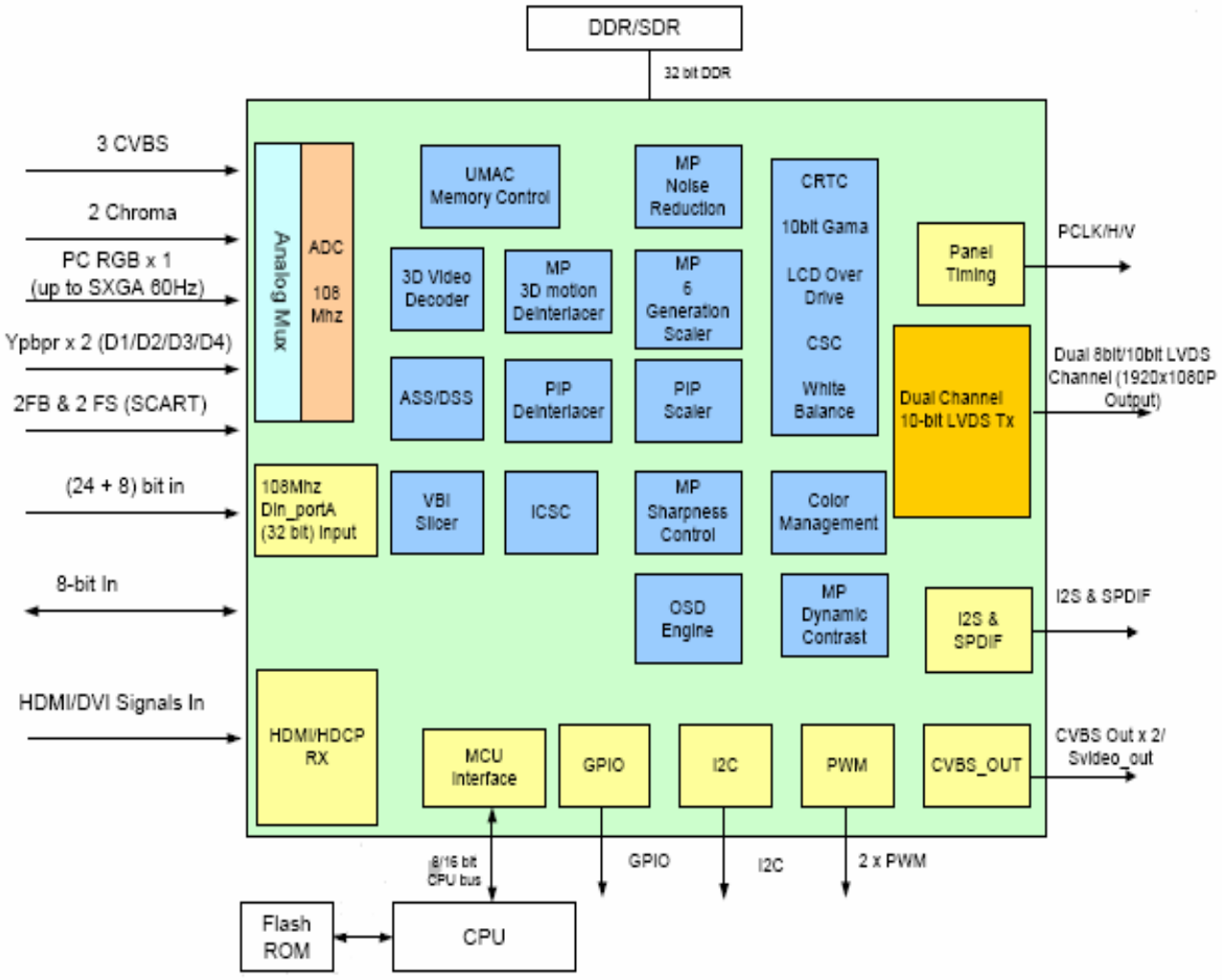


Figure 16: SVP LX66 Block Diagram

5.2. Video Matrix Switch: ST TEA6415

Description:

The main function of the TEA6415C is to switch 8 video input sources on the 6 outputs.
Each output can be switched to only one of the inputs, whereas any single input may be connected to several outputs. All switching possibilities are controlled through the

Features:

- 20 MHz bandwidth
- 8 inputs (CVBS, RGB, Chroma)
- 6 outputs
- Any single input may be connected to several outputs
- Bus controlled

- 6.5 dB gain between any input and output
- -55 dB crosstalk at 5 MHz
- Full ESD protection

Pin Configuration:

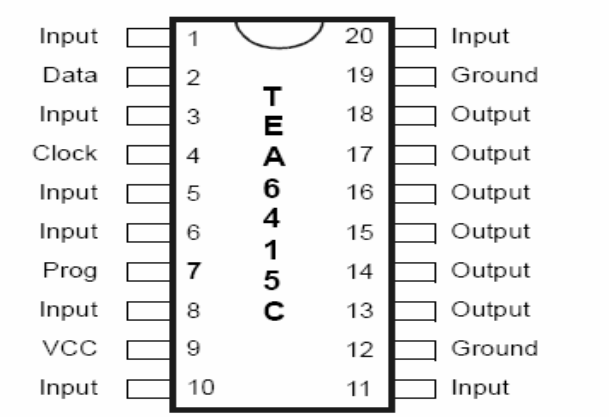


Figure 17: TEA 6415C Pin Configurations

Block Diagram:

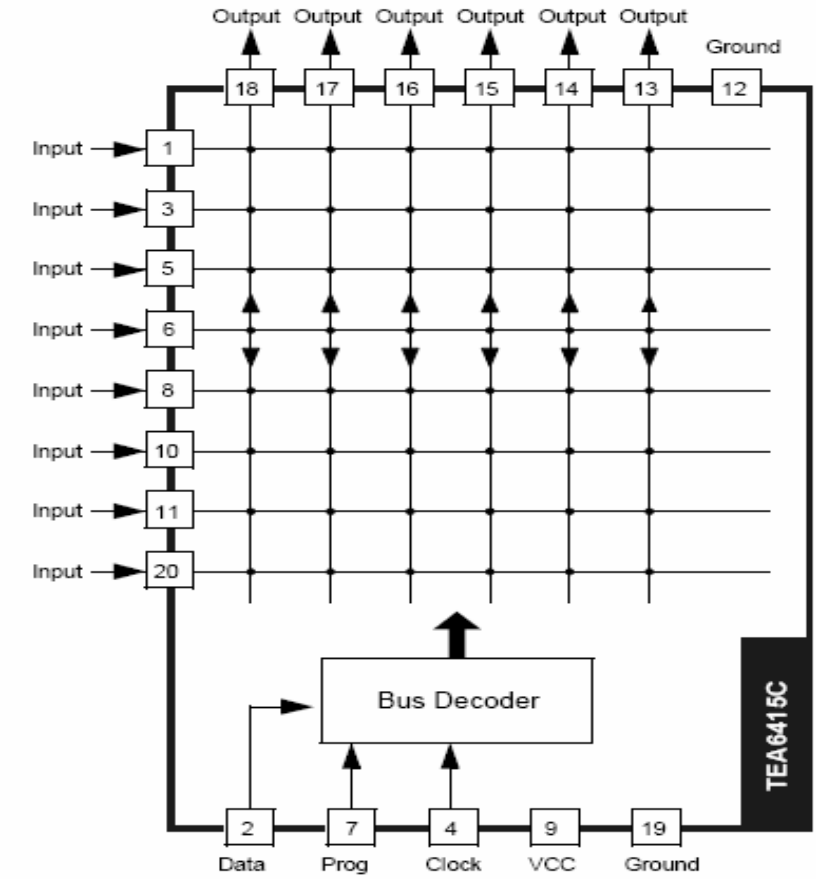


Figure 18: TEA 6415C Block Diagram

5.3. Video Decoder: Micronas VPC3230D

Description:

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. VPC3230D is used for PIP applications.

Features:

- adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard color decoder PAL/NTSC/SECAM including all substandards
- four CVBS, one S-VHS input, one CVBS output
- two RGB/YCrCb component inputs, one Fast Blank (FB) input
- integrated A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling 'Panoramavision'
- PAL+ preprocessing
- line-locked clock, data and sync, or 656-output interface
- peaking, contrast, brightness, color saturation and tint for RGB/YCrCb and CVBS/S-VHS
- high-quality soft mixer controlled by Fast Blank
- I2C-bus interface

Block Diagram:

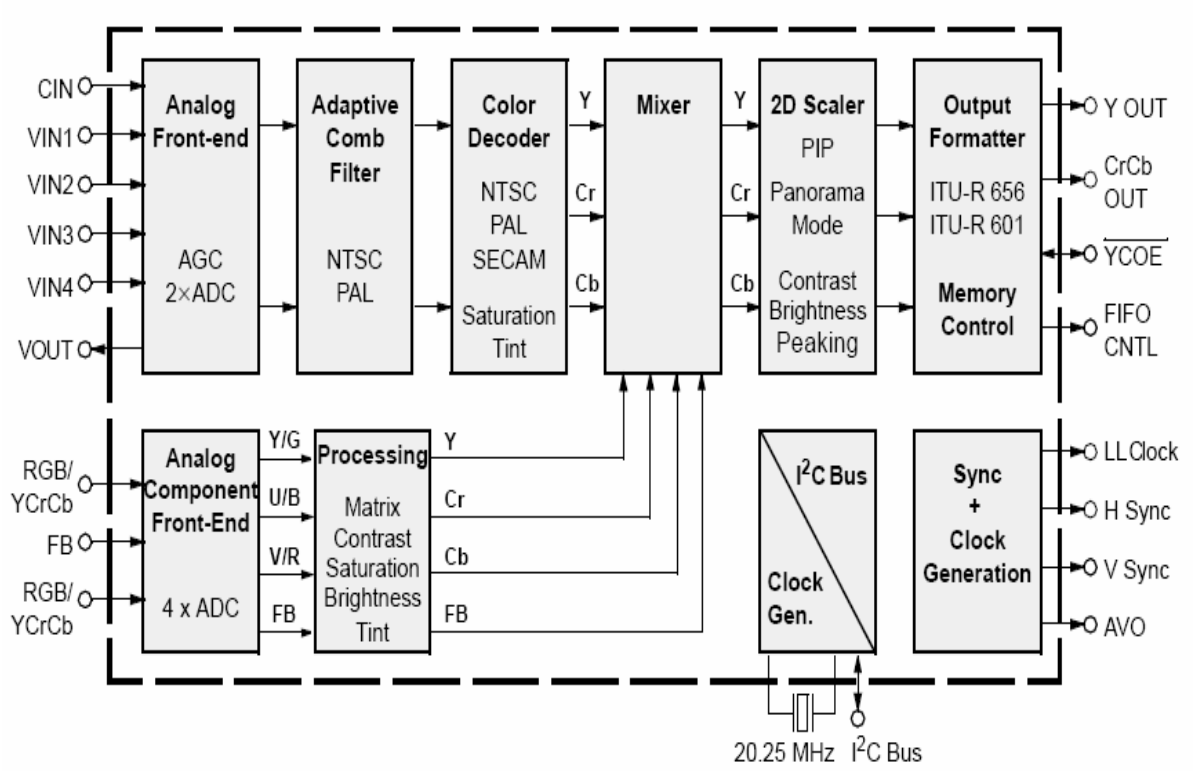


Figure 19: VPC3230D Block Diagram

5.4. Video RGB Switch: Pericom PI5V330

Description:

The PI5V330A is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications.

Features:

- Wide bandwidth: 400 MHz (typical)
- Low On-Resistance: 5Ω (typical)
- Low crosstalk at 10 MHz: –56dB
- Ultra-low quiescent power (0.1µA typical)

Pin Configurations:

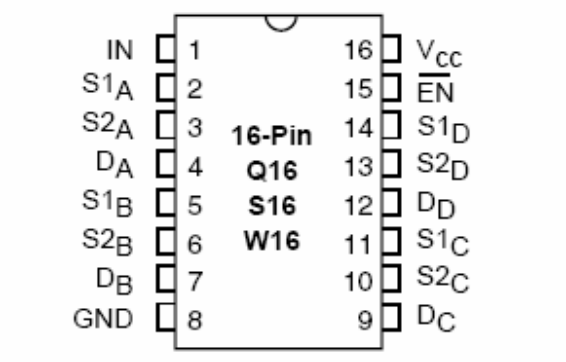


Figure 20: PI5V330 Pin Configurations

Pin Name	Description
$S1_A$, $S1_B$, $S1_C$, $S1_D$, $S2_A$, $S2_B$, $S2_C$, $S2_D$	Analog Video I/O
IN	Select Input
$\overline{EN}$	Enable
D_A, D_B, D_C, D_D	Analog Video I/O
GND	Ground
V_{CC}	Power

Table 7: PI5V330 Pin Descriptions

Block Diagram:

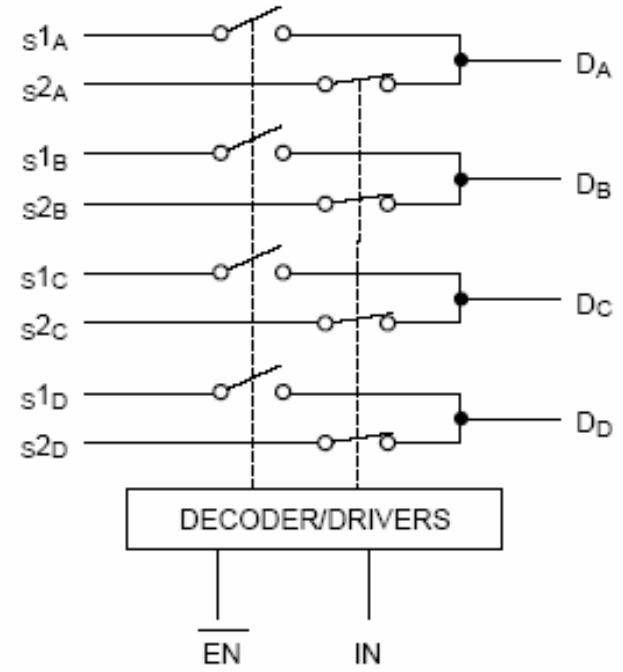


Figure 21: PI5V330 Block Diagram

6. HDMI BLOCK

6.1. HDMI Switch: AD8190

Description:

The AD8190 is an HDMI/DVI switch featuring equalised TMDS inputs and pre-emphasised TMDS outputs, ideal for systems with long cable runs. Outputs can be set to a high impedance state to reduce the power dissipation and/or allow the construction of larger arrays using the wire-OR technique.

The AD8190 is provided in a space saving, 56-lead, LFCSP, surface-mount, Pb-free, plastic package and is specified to operate over the −40°C to +85°C temperature range.

Features:

- Two inputs, one output HDMI/DVI links
- Enables HDMI 1.2a-compliant receiver
- Four TMDS channels per link

- Supports 250 Mbps to 1.65 Gbps data rates
- Supports 25 MHz to 165 MHz pixel clocks
- Equalised inputs for operation with long HDMI cables (20 metres at 1080p)
- Fully buffered unidirectional inputs/outputs
- Globally switchable 50Ω on-chip terminations
- Pre-emphasised outputs
- Low added jitter
- Single-supply operation (3.3 V)
- Four auxiliary channels per link
- Bidirectional unbuffered inputs/outputs
- Flexible supply operation (3.3 V to 5 V)
- HDCP standard compatible
- Allows switching of DDC bus and two additional signals
- Output disable feature
- Reduced power dissipation
- Output termination removal
- Two AD8190s support HDMI/DVI dual-link
- Standards compliant: HDMI receiver, HDCP, DVI
- Serial (I2C slave) control interface
- 56-lead, 8 mm x 8 mm, LFCSP, Pb-free package

Block Diagram:

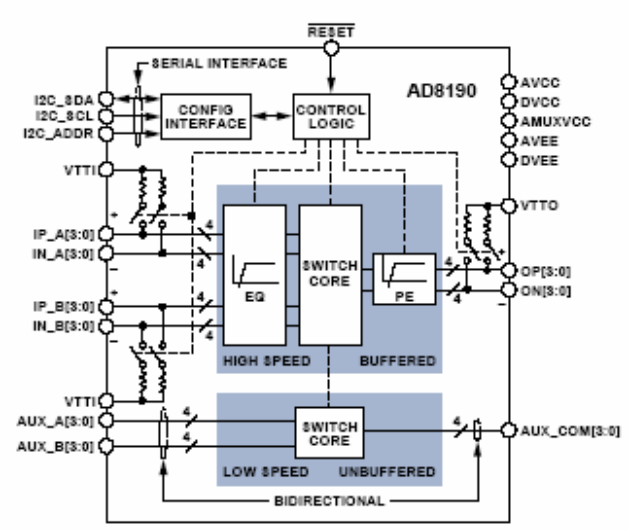


Figure 22: AD8190 Block Diagram

Pin Configuration:

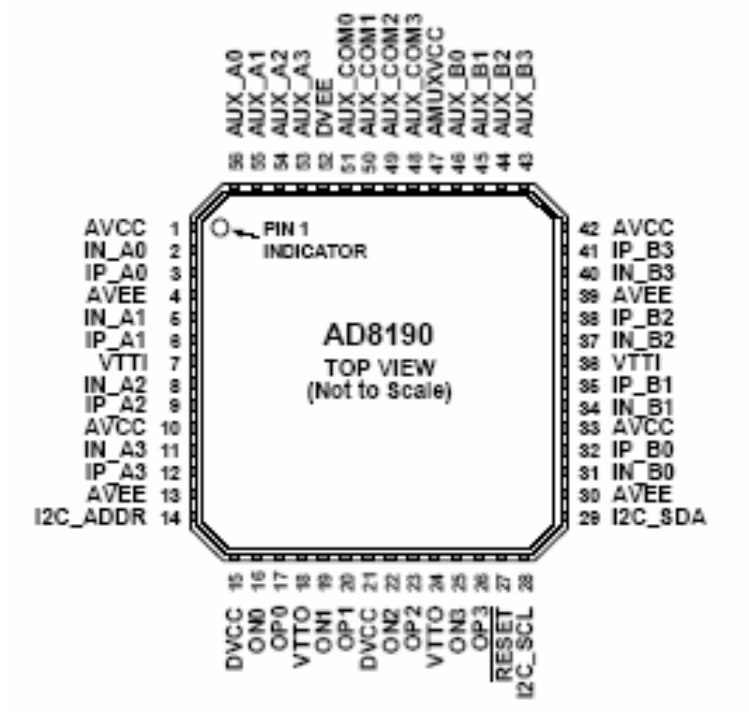


Figure 23: AD8190 Pin Configurations

Pin No.	Mnemonic	Type[1]	Description
1, 10, 33, 42	AVCC	Power	Positive Analog Supply. 3.3 V nominal.
2	IN_A0	HS I	High Speed Input Complement.
3	IP_A0	HS I	High Speed Input.
4, 13, 30, 39, ePAD	AVEE	Power	Negative Analog Supply. 0 V nominal.
5	IN_A1	HS I	High Speed Input Complement.
6	IP_A1	HS I	High Speed Input.
7, 36	VTTI	Power	Input Termination Supply. Nominally connected to AVCC.
8	IN_A2	HS I	High Speed Input Complement.
9	IP_A2	HS I	High Speed Input.
11	IN_A3	HS I	High Speed Input Complement.
12	IP_A3	HS I	High Speed Input.
14	I2C_ADDR	Control	I²C Address LSB.
15, 21	DVCC	Power	Positive Digital Power Supply. 3.3 V nominal.
16	ON0	HS O	High Speed Output Complement.
17	OP0	HS O	High Speed Output.
18, 24	VTTO	Power	Output Termination Supply. Nominally connected to AVCC.
19	ON1	HS O	High Speed Output Complement.
20	OP1	HS O	High Speed Output.
22	ON2	HS O	High Speed Output Complement.
23	OP2	HS O	High Speed Output.
25	ON3	HS O	High Speed Output Complement.
26	OP3	HS O	High Speed Output.
27	$\overline{\text{RESET}}$	Control	Configuration Registers Reset. This pin is normally pulled up to DVCC.
28	I2C_SCL	Control	I²C Clock.
29	I2C_SDA	Control	I²C Data.
31	IN_B0	HS I	High Speed Input Complement.
32	IP_B0	HS I	High Speed Input.
34	IN_B1	HS I	High Speed Input Complement.
35	IP_B1	HS I	High Speed Input.
37	IN_B2	HS I	High Speed Input Complement.
38	IP_B2	HS I	High Speed Input.
40	IN_B3	HS I	High Speed Input Complement.
41	IP_B3	HS I	High Speed Input.
43	AUX_B3	LS I/O	Low Speed Input/Output.
44	AUX_B2	LS I/O	Low Speed Input/Output.
45	AUX_B1	LS I/O	Low Speed Input/Output.
46	AUX_B0	LS I/O	Low Speed Input/Output.
47	AMUXVCC	Power	Positive Auxiliary Switch Supply. 5 V typical.
48	AUX_COM3	LS I/O	Low Speed Common Input/Output.
49	AUX_COM2	LS I/O	Low Speed Common Input/Output.
50	AUX_COM1	LS I/O	Low Speed Common Input/Output.
51	AUX_COM0	LS I/O	Low Speed Common Input/Output.
52	DVEE	Power	Negative Digital and Auxiliary Switch Power Supply. 0 V nominal.
53	AUX_A3	LS I/O	Low Speed Input/Output.
54	AUX_A2	LS I/O	Low Speed Input/Output.
55	AUX_A1	LS I/O	Low Speed Input/Output.
56	AUX_A0	LS I/O	Low Speed Input/Output.

Table 8: AD8190 Pin Descriptions

6.2. EEPROM for HDMI DDC: 24LC02

Description:

The Microchip Technology Inc. 24AA02/24LC02B (24XX02*) is a 2 Kbit Electrically Erasable PROM. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1 uA and 1 mA, respectively. The 24XX02 also has a page write capability for up to 8 bytes of data. The 24XX02 is available in the standard 8-pin PDIP, surface mount OIC, TSSOP and MSOP packages and is also available in the 5-lead SOT-23 package.

Features:

• Single supply with operation down to 1.8V
• Low-power CMOS technology
- 1 mA active current typical
- 1μA standby current typical (I-temp)
• Organised as 1 block of 256 bytes (1 x 256 x 8)
• 2-wire serial interface bus, I2C™ compatible
• Schmitt Trigger inputs for noise suppression
• Output slope control to eliminate ground bounce
• 100 kHz (24AA02) and 400 kHz (24LC02B) compatibility
• Self-timed write cycle (including auto-erase)
• Page write buffer for up to 8 bytes
• 2 ms typical write cycle time for page write
• Hardware write-protect for entire memory
• Can be operated as a serial ROM
• Factory programming (QTP) available
• ESD protection > 4,000V
• 1,000,000 erase/write cycles
• Data retention > 200 years
• 8-lead PDIP, SOIC, TSSOP and MSOP packages
• 5-lead SOT-23 package
• Pb-free finish available
• Available for extended temperature ranges:
- Industrial (I): -40°C to +85°C
- Automotive (E): -40°C to +125°C

Block Diagram:

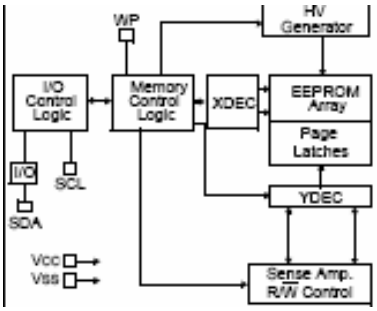


Figure 24: 24LC02 Block Diagram

Pin Configuration:

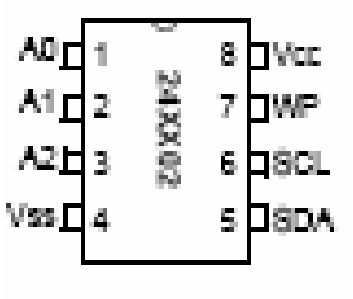


Figure 25: 24LC02 Pin Configuration

6.3. EEPROM FOR PC DDC: ST24LC21

Description:

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organised by 8 Bits.This device can operate in two modes: Transmit Only mode and I2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 cannot switch from the I2C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Features:

- 1 Mill on Erase/Write Cycles
- 40 Years Data Retent on
- 2.5v To 5.5v Single Supply Voltage
- 400kHz Compatibility Over The Full
- Range Of Supply Voltage
- Two W re Ser al Interface I2c Bus
- Compatible
- Page Write (Up To 8 Bytes)
- Byte, Random And Sequent al Read
- Modes
- Self Timed Programm ng Cycle
- Automatic Address Incrementing
- Enhanced Esd/Latch Up
- Performances

Pin Configuration:

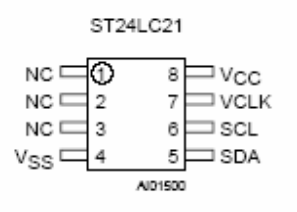


Figure 26. 24LC21 pin configuration

7. REGULATOR ICS

7.1. LM317

Description:

The LM117/LM217/LM317 are monolithic integrated circuit in TO-220, TO-220FP, TO-3 and D2PAK packages intended for use as positive adjustable voltage regulators. They are designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range. The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed regulators.

Features:

- Output voltage range:1.2 to 37V
- Output current in excess of 1.5A
- 0.1% line and load regulation
- Floating operation fro high voltages
- Complete series of protections: Current limiting, thermal shutdown and SOA control

Pin Configuration:

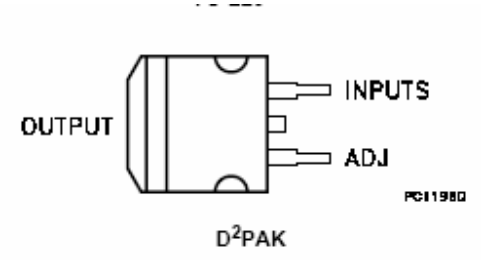


Figure 27: LM317 Pin Configuration

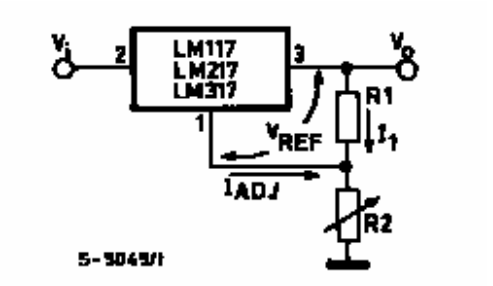


Figure 28: LM317 Application Circuit

7.2. LM1117 800mA Low-Dropout Linear Regulator

Description:

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10μF tantalum capacitor is required at the output to improve the transient response and stability.

Features:

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Temperature Range 0°C to 125°C
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)

Pin Configuration:

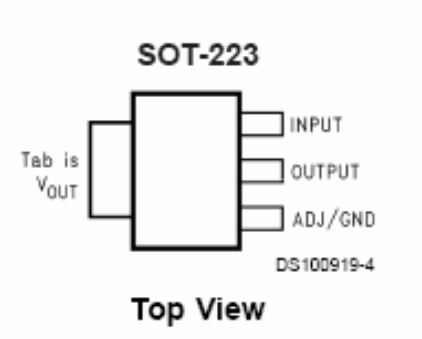


Figure 29: LM1117 Pin Configuration

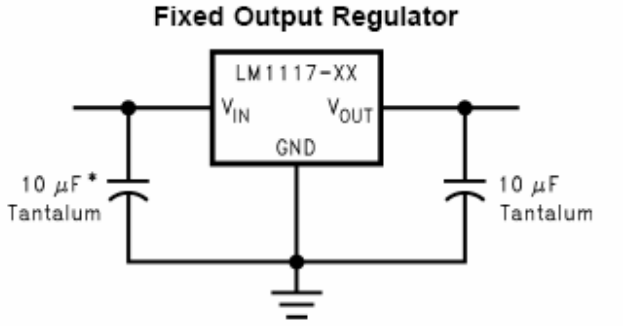


Figure 30: LM1117 Application Circuit

7.3. IDT74LVC14A HEX Schmitt Trigger Inverter

Description:

This IC is used to detect the PC standby.The LVC14A Hex Schmitt Trigger inverter is built using advanced dual metal CMOS technology. This device contains six independent inverters and performs the Boolean function Y = A. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system. The LVC14A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Features:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
- 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP and
- 0.65mm pitch TSSOP packages
- Extended commercial range of – 40°C to +85°C
- VCC = 3.3V ±0.3V, Normal Range
- VCC = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Pin Configuration:

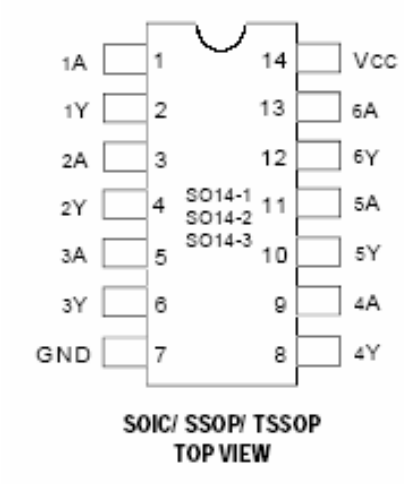


Figure 31: IDT74LVC14A Pin Configuration

Pin Names	Description
xA	Inputs
xY	Outputs

Inputs	Outputs
xA	xY
H	L
L	H

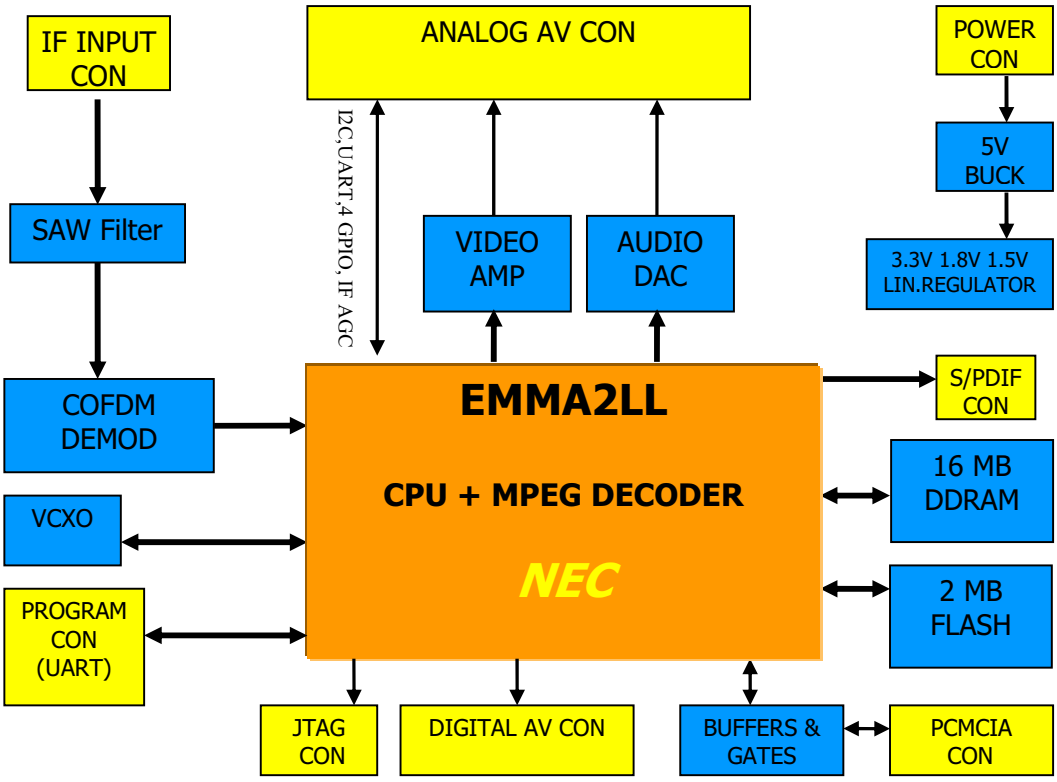
NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level

Table 9: IDT74LVC14A Pin Description

8. TDM1300 HARDWARE DESCRIPTION

Item	Description
PCB	4 layer
MPEG decoder	EMMA2LL (NEC)
FLASH	29LV160TE (Spansion, Eon) 2MB
DDRAM	EDD1216AATA (Elpida, Nanya) 16MB
Audio DAC	CS4335 (Crystal)
Video AMP	FMS6145 (Fairchild)
COFDM Demodulator	DRX3973D (Micronas)
Tuner	DTT7103 (Thomson) DTOS401TH17XA (Samsung)
VCXO	PI6CX100-27 (Pericom)
Buck Regulator	MP1593 (MPS)
3.3V Regulator	NCP1117-3.3V (Onsemi)
1.8V Regulator	NCP1117-1.8V (Onsemi)
1.5V Regulator	NCP1117-1.5V (Onsemi)
74LVC16244 (x4)	16 bit buffer with OE (Various)
74LVC245	Octal Bus Transceiver (Various)
74LVC00	NAND Gate (Various)

9. IDTV MODULE BLOCK DIAGRAM



10. CONNECTORS

10.1 POWER Connector:

Pin	Description
1	+12/24V
2	+12/24V
3	GND
4	GND

10.2 EMMA2LL JTAG Connector:

Pin	Description
1	GND
2	JTCLK
3	3.3V
4	JTDO
5	NC
6	JTMS
7	NC
8	JTRST
9	GND
10	JTDI

10.3 ANALOG AV Connector:

Pin	Description	Pin	Description
1	DVB_SCL	13	GND
2	DVB_SDA	14	GND
3	GND	15	DVB_R_AUDIO
4	GND	16	DVB_L_AUDIO
5	IRQ	17	GND
6	DVB_RX	18	DVB_IN_CVBS
7	DVB_TX	19	GND
8	GPIO4	20	DVB_IN_B / DVB_IN_C
9	GPIO3	21	GND
10	GPIO2	22	DVB_IN_G / DVB_IN_Y
11	GPIO1	23	GND
12	IF_AGC_DVB	24	DVB_IN_R

10.4 IF Connector:

Pin	Description
1	IF +
2	IF -
3	GND

10.5 PROGRAMMING Connector:

Pin	Description
1	TXD
2	GND
3	RXD

10.6 S/PDIF Connector:

Pin	Description
1	S/PDIF
2	GND

10.7 DIGITAL AV Connector:

Pin	Description	Pin	Description
1	I2S Word Select	11	GND
2	I2S Serial Clock	12	Digital Video Pixel Clock
3	I2S Serial Data	13	Digital Video Y/Cb/Cr DATA7
4	GND	14	Digital Video Y/Cb/Cr DATA6
5	GND	15	Digital Video Y/Cb/Cr DATA5
6	GND	16	Digital Video Y/Cb/Cr DATA4
7	Internal Vertical SYNC	17	Digital Video Y/Cb/Cr DATA3
8	Internal Horizontal SYNC	18	Digital Video Y/Cb/Cr DATA2
9	GND	19	Digital Video Y/Cb/Cr DATA1
10	GND	20	Digital Video Y/Cb/Cr DATA0

10.8 PCMCIA Connector:

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	**35**	GND	Ground
2	D3	Data bit 3	**36**	CD1#	Card Detect
3	D4	Data bit 4	**37**	MDO3	MPEG Data Out 3
4	D5	Data bit 5	**38**	MDO4	MPEG Data Out 4
5	D6	Data bit 6	**39**	MDO5	MPEG Data Out 5
6	D7	Data bit 7	**40**	MDO6	MPEG Data Out 6
7	CE1#	Card Enable	**41**	MDO7	MPEG Data Out 7
8	A10	Address bit 10	**42**	CE2#	Card Enable
9	OE#	Output Enable	**43**	VS1#	Voltage Sense 1
10	A11	Address bit 11	**44**	IORD#	I/O Read
11	A9	Address bit 9	**45**	IOWR#	I/O Write
12	A8	Address bit 8	**46**	MISTRT	MPEG Data In Start
13	A13	Address bit 13	**47**	MDI0	MPEG Data In 0
14	A14	Address bit 14	**48**	MDI1	MPEG Data In 1
15	WE#	Write Enable	**49**	MDI2	MPEG Data In 2
16	IREQ#	Interrupt Request	**50**	MDI3	MPEG Data In 3
17	VCC	Supply Voltage	**51**	VCC	Supply Voltage
18	VPP	Programming and Peripheral Supply	**52**	VPP	Programming and Peripheral Supply
19	MIVAL	MPEG Data In Valid	**53**	MDI4	MPEG Data In 4
20	MCLKI	MPEG Data Clock Input	**54**	MDI5	MPEG Data In 5
21	A12	Address bit 12	**55**	MDI6	MPEG Data In 6
22	A7	Address bit 7	**56**	MDI7	MPEG Data In 7
23	A6	Address bit 6	**57**	MCLKO	MPEG Data Clock Output
24	A5	Address bit 5	**58**	RESET	Card Reset
25	A4	Address bit 4	**59**	WAIT#	Extend bus cycle
26	A3	Address bit 3	**60**	INPACK#	Input Port Acknowledge
27	A2	Address bit 2	**61**	REG#	Register select & I/O Enable
28	A1	Address bit 1	**62**	MOVAL	MPEG Data Out Valid
29	A0	Address bit 0	**63**	MOSTRT	MPEG Data Out Start
30	D0	Data bit 0	**64**	MDO0	MPEG Data Out 0
31	D1	Data bit 1	**65**	MDO1	MPEG Data Out 1
32	D2	Data bit 2	**66**	MDO2	MPEG Data Out 2
33	IOIS16#	I/O Port Is 16-bit	**67**	CD2#	Card Detect
34	GND	Ground	**68**	GND	Ground

11. SERVICE MENU SETTINGS

To enter the service menu, first enter the MENU by pressing "**MENU**" button and then press the digits 1, 4, 6 and 1 respectively.

11.1. Picture Adjust

• *Source => All possible sources given with the chassis as a list.*

• *Mode => Three items as a list; NATURAL, DYNAMIC, CINEMA*

• *Colour Temp => Three items as a list; COOL, NORMAL, WARM*

• *Contrast => Slider Bar. Changing value between 0 to 63. Default is 63.*

• *Brightness => Slider Bar. Changing value between 0 to 63. Default is 32.*

• *Sharpness => Slider Bar. Changing value between 0 to 31. Default is 22.*

• *Colour => Slider Bar. Changing value between 0 to 99. Default is 70.*

• *R => Slider Bar. Changing value between 0 to 31. Default is 31.*

• *G => Slider Bar. Changing value between 0 to 31. Default is 31.*

• *B => Slider Bar. Changing value between 0 to 31. Default is 31.*

• *Backlight => Slider Bar. Changing value between 0 to 255. Default is 30.*

In this menu preset values for each Mode (Contrast, Brightness, Sharpness, Colour values for each Mode-NATURAL, DYNAMIC, CINEMA) and for each Colour Temp. (R, G, B values for each Colour Temp- COOL, NORMAL, WARM) are determined for each source.

11.2. SOUND1

• *Menu Subwoofer => If ON, Subwoofer option is available in TV set, and the item is visible in sound menu, else Subwoofer is not available. Default is ON.*

• *Subwoofer Level (dB) => This value is gain value of Subwoofer output in dB. -30...12. Default is 0.*

• *Subwoofer Corner Freq. (x10Hz) => Last low frequency value that is amplified. 5...40. Default is 22.*

• *Menu Equalizer => If ON, visible in sound menu, else invisible.Default is ON.*

• *Menu Headphone => If ON, visible in sound menu, else invisible. Default is ON.*

• *Menu Effect => If ON, visible in sound menu, else invisible. Default is ON.*

• *Menu Wide Sound => If ON, visible in sound menu, else invisible. Default is ON.*

• *Menu Dynamic Bass => If ON, visible in sound menu, else invisible. Default is ON.*

• *Menu Virtual Dolby => If ON, visible in sound menu, else invisible. Default is ON.*

• *Carrier Mute => If ON, in the absence of an FM carrier the output is muted,else not. Default is ON.*

• Virtual Dolby Text => Active if VIRTUAL DOLBY is ON. According to the selection; seen in sound menu as 3D PANORAMA or VIRTUAL DOLBY. Default is 3DS.

11.3. SOUND 2

• AVL => AVL is controlled from this menu by service user, ON/OFF. Default is ON.

• Menu AVL => If ON, AVL item is visible in sound menu, and AVL can be controlled from sound menu by normal user, else AVL is invisible to normal user. Default is ON.

• FM PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for the related standard. 0...127. Default is 15.

• NICAM PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for the related standard. 0...127. Default is 34.

• SCART PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for scart outputs. 0...127. Default is 15.

• SCART VOLUME AVL ON => If AVL ON, set value in this item is used as volume value for scart1 and scart2. 0...127. Default is 122.

• FM PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for the related standard. 0...127. Default is 15.

• NICAM PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for the related standard. 0...127. Default is 34.

• SCART PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for scart outputs. 0...127. Default is 15.

• SCART VOLUME AVL OFF => If AVL OFF, set value in this item is used as volume value for scart1 and scart2. 0...127. Default is 122.

• I2S prescale=> *set value in this item is used as prescale value for HDMI outputs* 0..255. *Default is 5.*

11.4. Options

• Burn-In Mode => If ON, When TV is powered ON Green, Blue, Red is displayed in sequence until Menu button is pressed. Default is OFF.

• FIRST APS => If ON, "First APS" menu is displayed when the TV is switched on with the factory default settings. Default is OFF.

• APS Volume => After First APS function finishes, the volume of the TV is that value. Default is 15.

• AGC (dB) => Tuner AGC value. Default is 8.

• Power-Up Mode => Mode defines the TV set power on state. Default is standby.
Stand-by : When TV is ON set is in stand-by mode
Normal : When TV is ON set is in normal mode
Last State: When TV is ON set is in Last State mode

• Factory Reset => OK to activate. When OK is pressed on this item, factory defaults loaded.

• Enter Flash Mode=>

• Reset Eeprom => Initialise default settings.

• Remote select=> 0=RC1546

1=RC1549/1602/1082/1055
2=RC1062
3=RC1072
4=RC1558
5=RC1061
6=RC1071
7=RC1110
8=RK18

Default is 2.

11.5. TV Norm

• *BG => If ON, this standard is supported, else not supported. Default is ON.*

• *DK => If ON, this standard is supported, else not supported. Default is ON.*

• *I => If ON, this standard is supported, else not supported. Default is ON.*

• *L => If ON, this standard is supported, else not supported. Default is ON.*

• *LP => If ON, this standard is supported, else not supported. Default is ON.*

• *M => If ON, this standard is supported, else not supported. Default is ON.*

11.6. Features

• PIP/PAP => If ON enables the PIP/PAP. *Default is ON.*

• *Blue Background => If ON, Blue Background is visible in Feature Menu else not. Default is ON.*

• *Menu Transparency => If ON, Menu Transparency is visible in Feature Menu else not. Default is ON.*

• *Menu Timeout => If ON, Menu Timeout is visible in Feature Menu else not. Default is OFF.*

• *Backlight => If ON, Backlight is visible in Feature Menu else not. Default is OFF.*

• *Dynamic WB => Dynamic White Balance. Default is ON.*

• Zoom Mode Blank=> If ON, displays blank while changing the zoom mode else not. *Default is OFF.*

• Dynamic Menu=>If ON, the features covered by some patents will be used, else not.

11.7. Teletext

• *TOP TXT => If ON, Top Text feature is available else not. Default is ON.*

• *Fast TXT => If ON, Fast Text feature is available else not. Default is ON.*

• *Teletext Language => Teletext Language may be controlled from this menu by service user*

.

• *Menu Teletext Language => If ON, Teletext Language item is visible in Feature Menu, and Teletext Language can be controlled from Feature Menu by normal user, else Teletext Language is invisible to normal user. Default is ON.*

• Check Data=>Used to check the teletext data. No service usage.

11.8. Source

• *TV*

• *SC1*

• *SC2*

• *SC2 SVHS*

• *SC3*

• *SC3 SVHS*

• *YPBPR*

• *FAV*

• *SVHS*

• *HDMI*

• *HDMI2*

• *PC*

This menu is related with the options of the chassis. These items may be ON or OFF. If ON, the source is available in TV set, and the item is visible in source menu, else the source may be available but invisible to user.

Menu Languages 1 & 2

The language options for the Language item in Feature menu can be set ON or OFF from this menu.
English, German, French, Turkish, Spanish, Danish, Swedish, Dutch, Italian, Greek, Portuguese, Norwegian Finnish, Polish, Czech, Hungarian, Russian, Slovak, Slovenian, Rumanian, Bulgarian, Croatian, Serbian, Hebrew

11.9. Tuner options

•Main tuner=> The main tuner used in the TV is selected.

•PIP tuner=> The pip tuner used in the TV is selected.

11.10. Hotel Menu Settings

To enter the hotel menu, first enter the MENU by pressing "**MENU**" button and then press the digits 7, 9, 3 and 5 respectively.

• Hotel mode => If ON, hotel menu settings will be valid, else not.

• Startup position => The selected source will be active when the TV is on.

• Volume Level=> The set value will be the volume level when the TV is on and cannot be changed from the menu by the user.

• Front Key => ???

• Osd Menu => Determines the visibility of menus to the user according to the selection: Enable/Disable Install Menu/Disable All Menus

• Autosave => Update Last Data/Not Stored

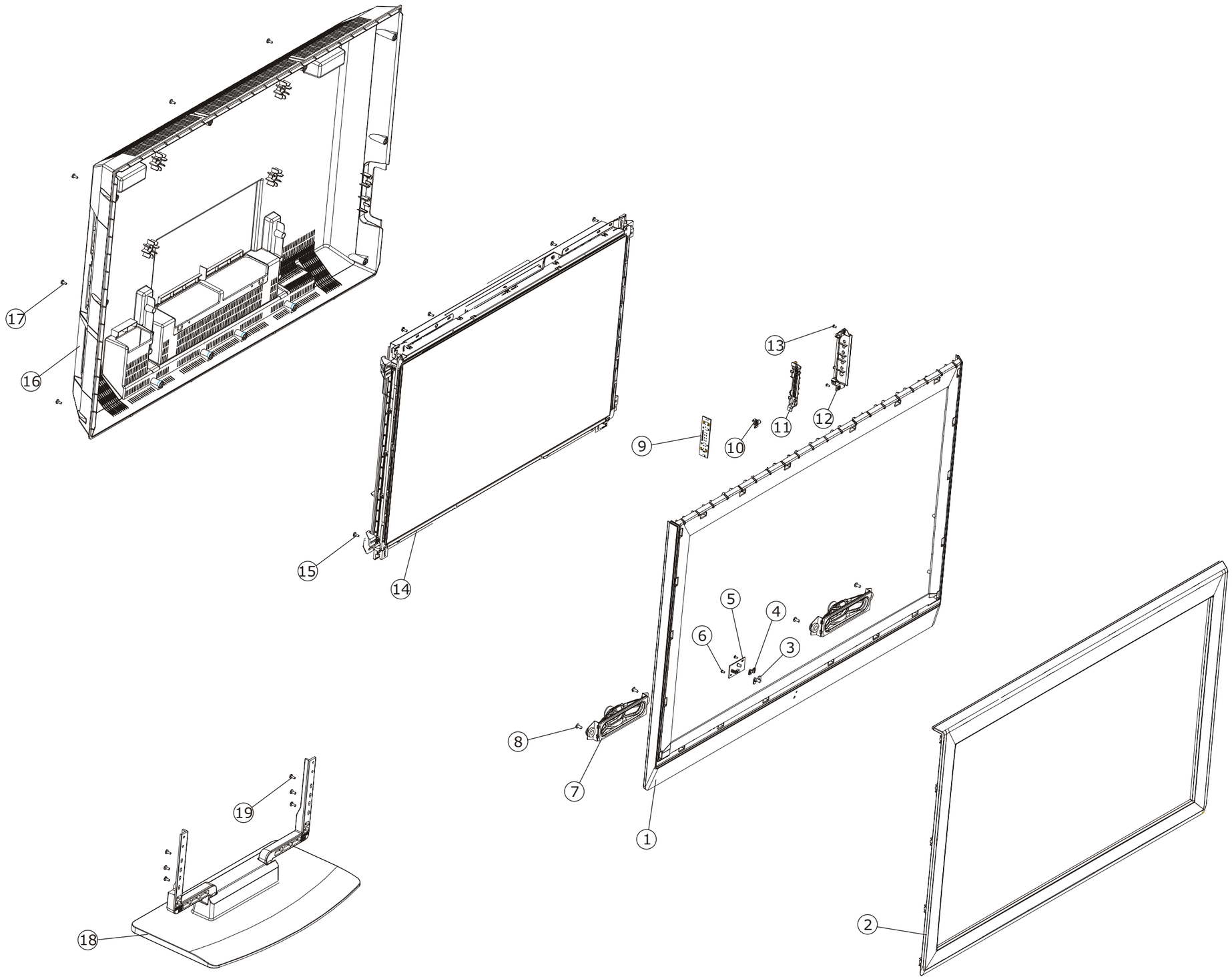
12. REPLACEMENT PARTS

THE UPDATED PARTS LIST

FOR THIS MODEL IS

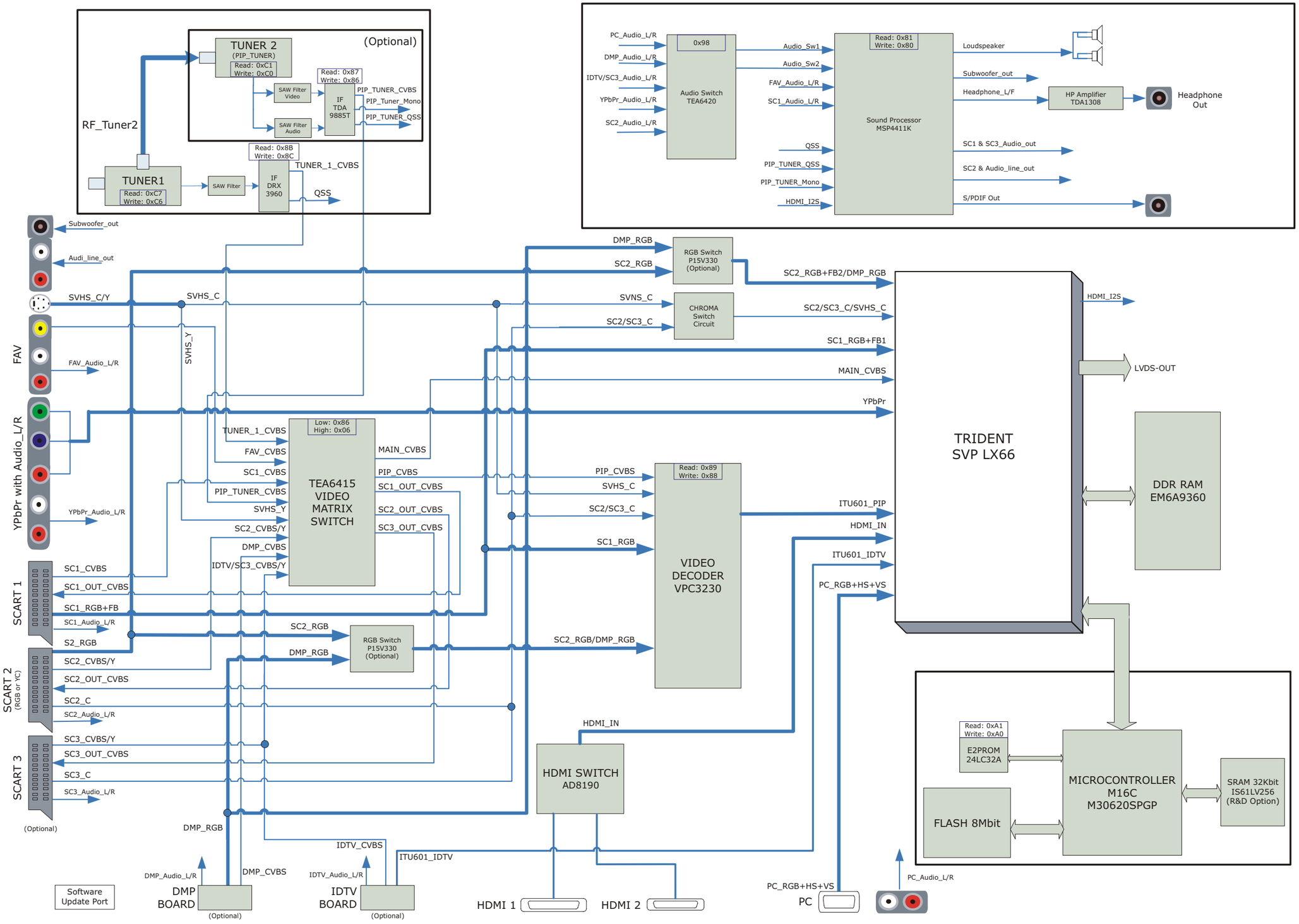
AVAILABLE ON ESTA

13. ASSEMBLY DIAGRAM



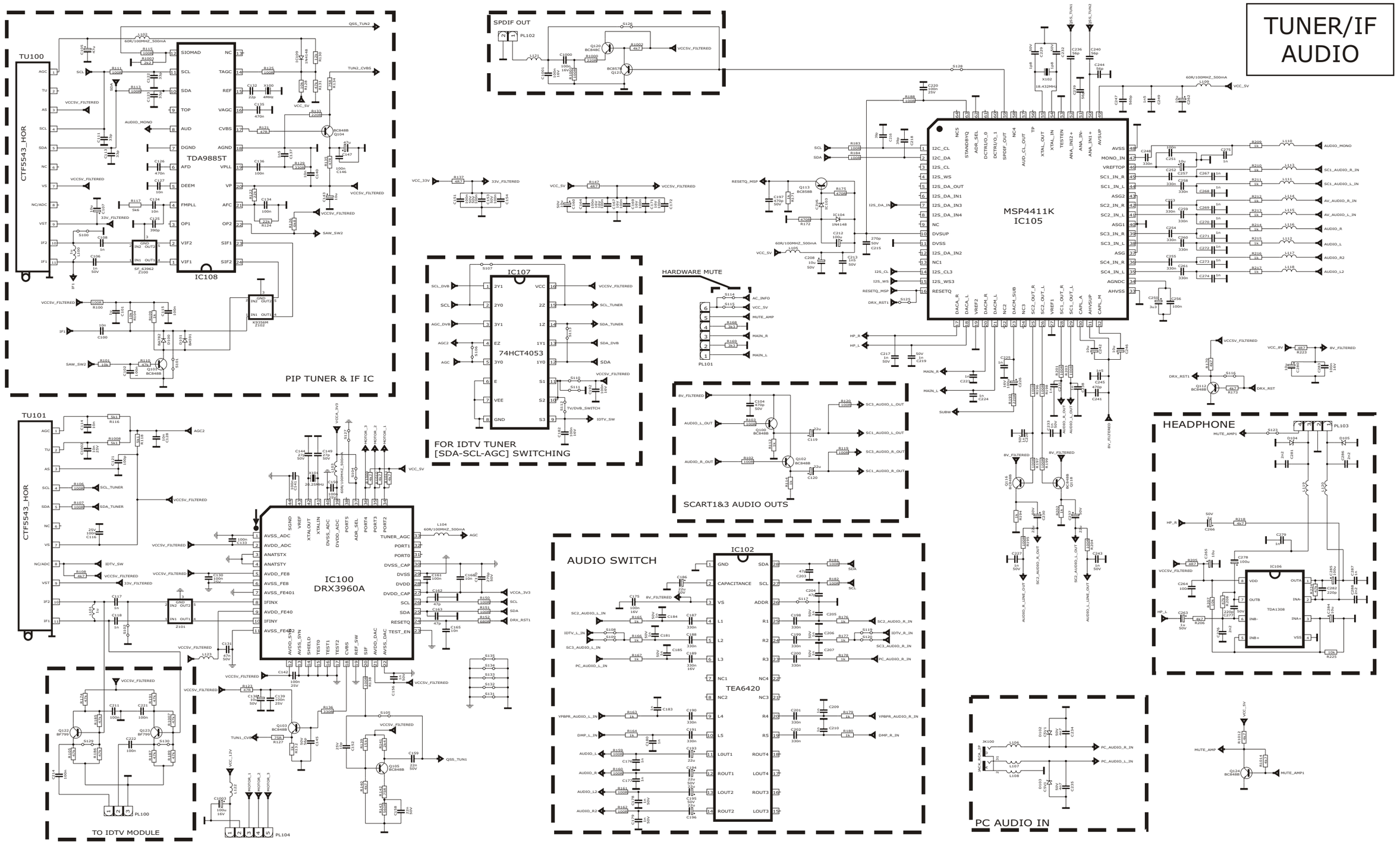
No. 0236	EXPLODED VIEW	HITACHI

14. BLOCK DIAGRAM

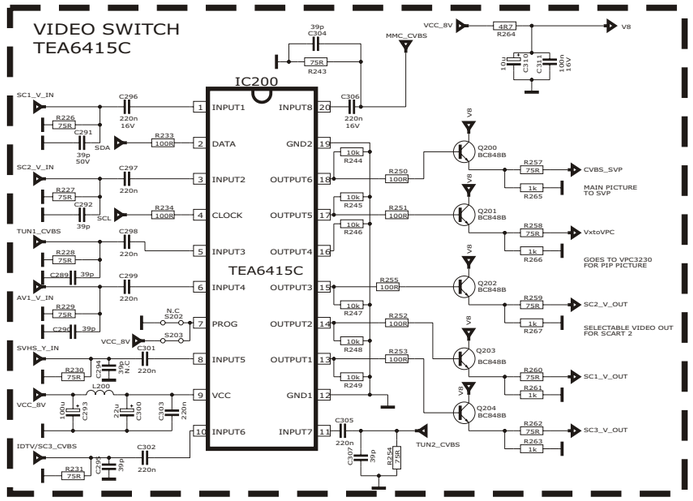


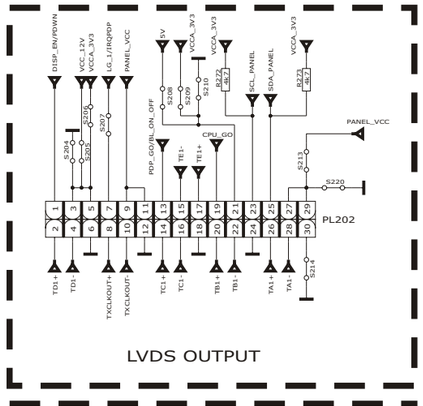
No. 0236	BLOCK DIAGRAM	HITACHI

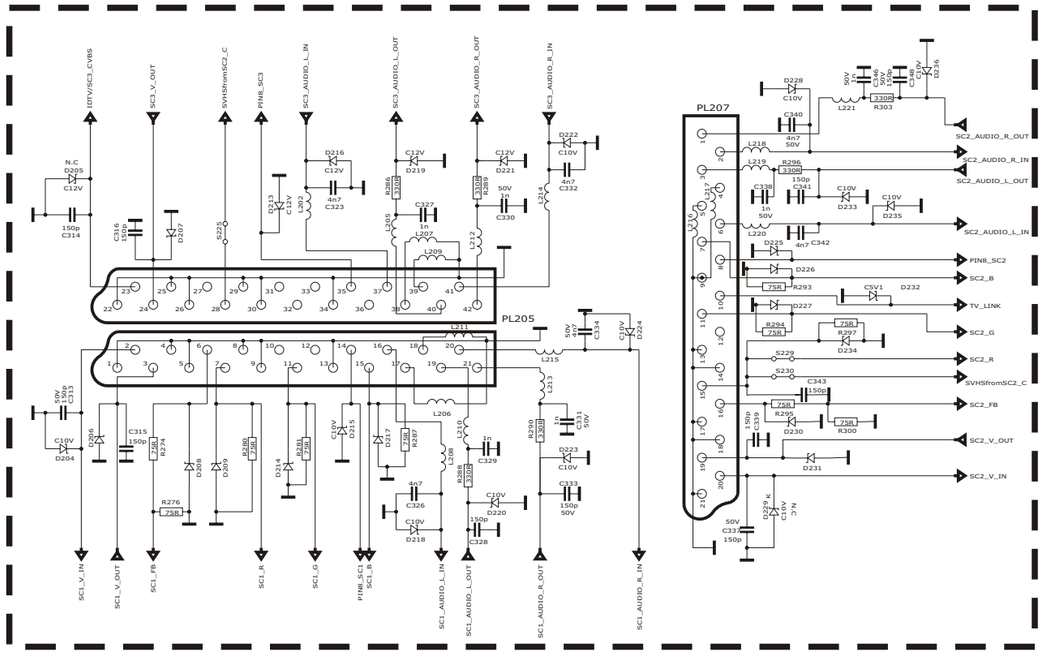
15. SCHEMATIC DIAGRAMS

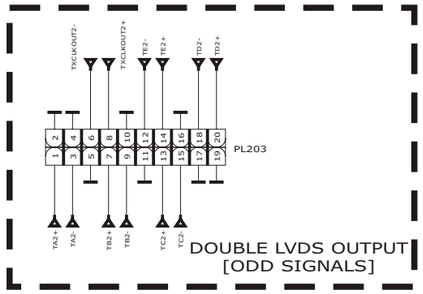


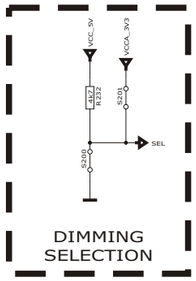
17MB26	MAIN BOARD CIRCUIT - SHEET 1	HITACHI

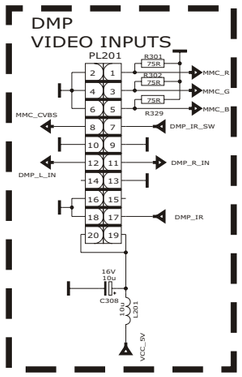

VIDEO SWITCH
TEA6415C
IC200
TEA6415C
INPUT1
INPUT2
INPUT3
INPUT4
INPUT5
INPUT6
DATA
CLOCK
PROG
VCC
GND1
GND2
INPUT8
OUTPUT6
OUTPUT5
OUTPUT4
OUTPUT3
OUTPUT2
OUTPUT1
INPUT7
SC1_V_IN
SC2_V_IN
TUN1_CVBS
AV1_V_IN
SVHS_Y_IN
VCC_8V
IDTV/SC3_CVBS
MMC_CVBS
TUN2_CVBS
CVBS_SVP
MAIN PICTURE TO SVP
VxtoVPC
GOES TO VPC3230 FOR PIP PICTURE
SC2_V_OUT
SELECTABLE VIDEO OUT FOR SCART 2
SC1_V_OUT
SC3_V_OUT

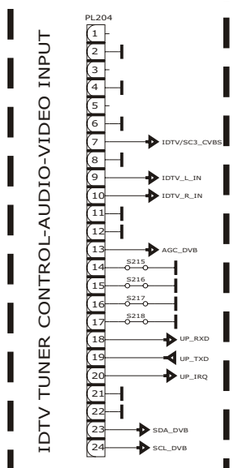

PL202
PANEL_VCC
LVDS OUTPUT

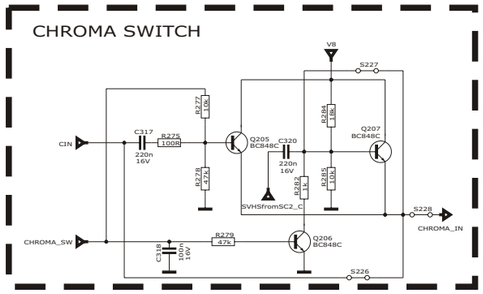

PL205
PL207
IDTV/SC3_CVBS
SC3_V_OUT
SVHSfromSC2_C
PIN8_SC3
SC3_AUDIO_L_IN
SC3_AUDIO_L_OUT
SC3_AUDIO_R_OUT
SC3_AUDIO_R_IN
SC1_V_IN
SC1_V_OUT
SC1_FB
SC1_R
SC1_G
PIN8_SC1
SC1_B
SC1_AUDIO_L_IN
SC1_AUDIO_L_OUT
SC1_AUDIO_R_OUT
SC1_AUDIO_R_IN
SC2_AUDIO_R_OUT
SC2_AUDIO_R_IN
SC2_AUDIO_L_OUT
SC2_AUDIO_L_IN
PIN8_SC2
SC2_B
TV_LINK
SC2_G
SC2_R
SVHSfromSC2_C
SC2_FB
SC2_V_OUT
SC2_V_IN

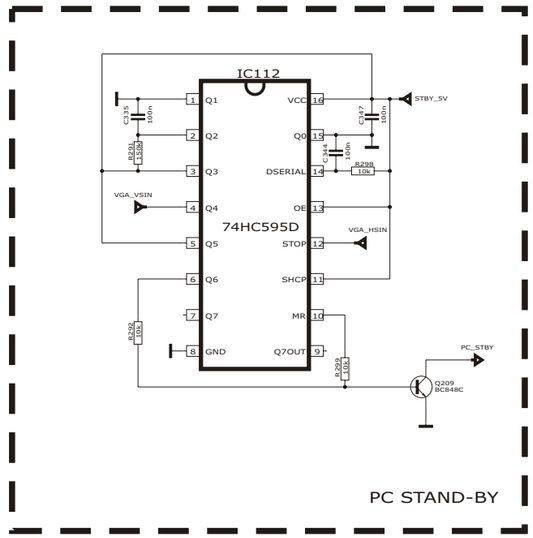

PL203
DOUBLE LVDS OUTPUT
[ODD SIGNALS]

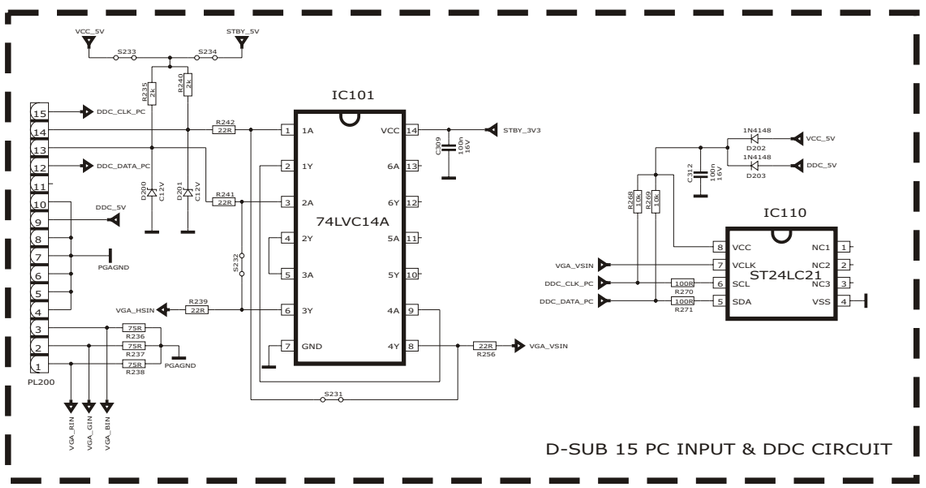

DIMMING
SELECTION


DMP
VIDEO INPUTS
PL201
MMC_CVBS
DMP_L_IN
MMC_R
MMC_G
MMC_B
DMP_IR_SW
DMP_R_IN
DMP_IR

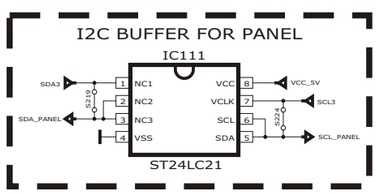

PL204
IDTV TUNER CONTROL-AUDIO-VIDEO INPUT
IDTV/SC3_CVBS
IDTV_L_IN
IDTV_R_IN
AGC_DVB
UP_RXD
UP_TXD
UP_IRQ
SDA_DVB
SCL_DVB

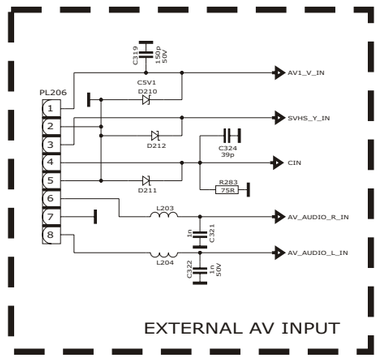

CHROMA SWITCH
CIN
CHROMA_SW
SVHSfromSC2_C
CHROMA_IN


IC112
74HC595D
VGA_VSIN
VGA_HSIN
STBY_5V
PC_STBY
PC STAND-BY


IC101
74LVC14A
PL200
DDC_CLK_PC
DDC_DATA_PC
DDC_5V
PGAGND
VGA_HSIN
STBY_3V3
VGA_VSIN
VGA_RIN
VGA_GIN
VGA_BIN
D-SUB 15 PC INPUT & DDC CIRCUIT

IC110
ST24LC21
VGA_VSIN
DDC_CLK_PC
DDC_DATA_PC
VCC_5V
DDC_5V

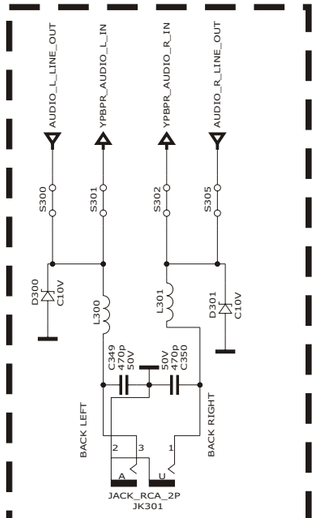

I2C BUFFER FOR PANEL
IC111
ST24LC21
SDA3
SDA_PANEL
VCC_5V
SCL3
SCL_PANEL


PL206
AV1_V_IN
SVHS_Y_IN
CIN
AV_AUDIO_R_IN
AV_AUDIO_L_IN
EXTERNAL AV INPUT

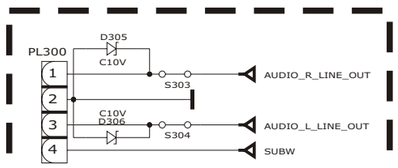
TV IN/OUT

TV
VPC3230 - PIP

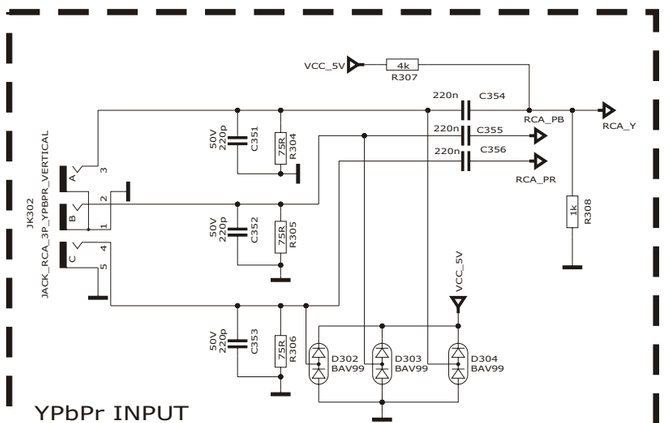
YPbPr AUDIO IN/ LINE OUT

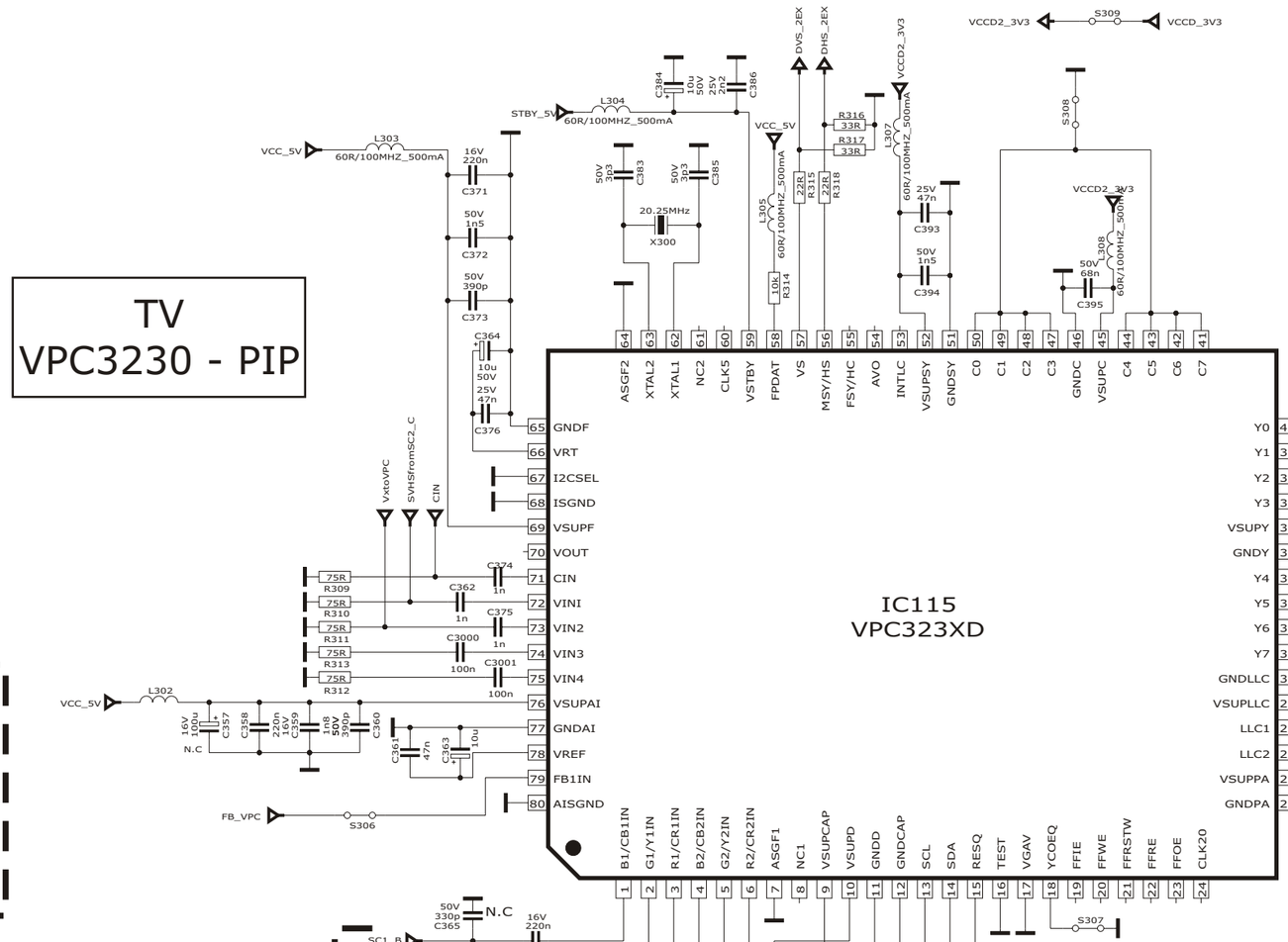


SIDE AV LINE OUT

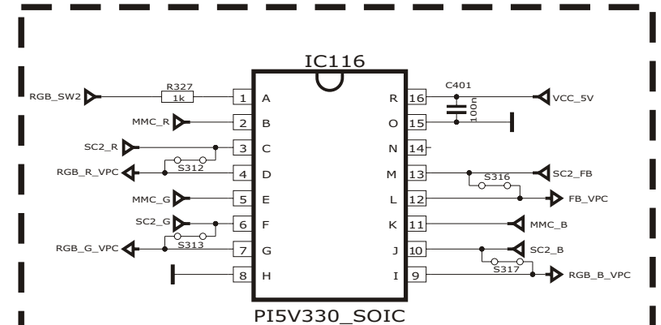


YPbPr INPUT

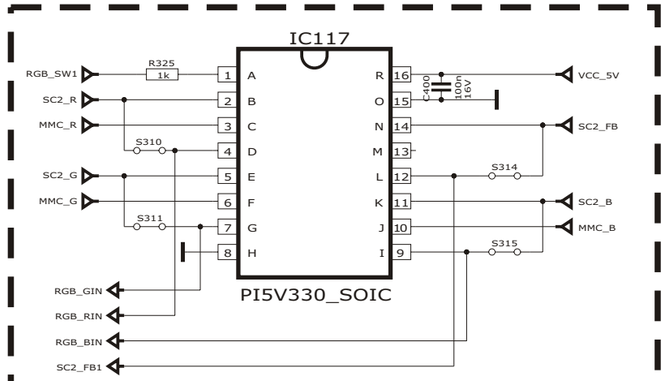




IC115
VPC323XD



RGB SWITCHING FOR VPC SC2/DMP



SC2/DMP RGB SWITCHING FOR SVP

17MB26	MAIN BOARD CIRCUIT - SHEET 3	HITACHI

VIDEO DEC-LVDS-SCALER IC

IC1

SVP_LX_66

SIGNAL TERMINATION

PC INPUT

IDTV DIGITAL INTERFACE [FFC TYPE]

PIP INPUT

IDTV INPUTS

DOUBLE LVDS OUT

SINGLE LVDS OUT

CMO PANEL OPTION FOR 2ND LVDS

CMO PANEL OPTION

SC2_RGB/DMP INPUT

YPbPr INPUT

SC1_RGB INPUT

VGA INPUT

SCART RGB DETECTION

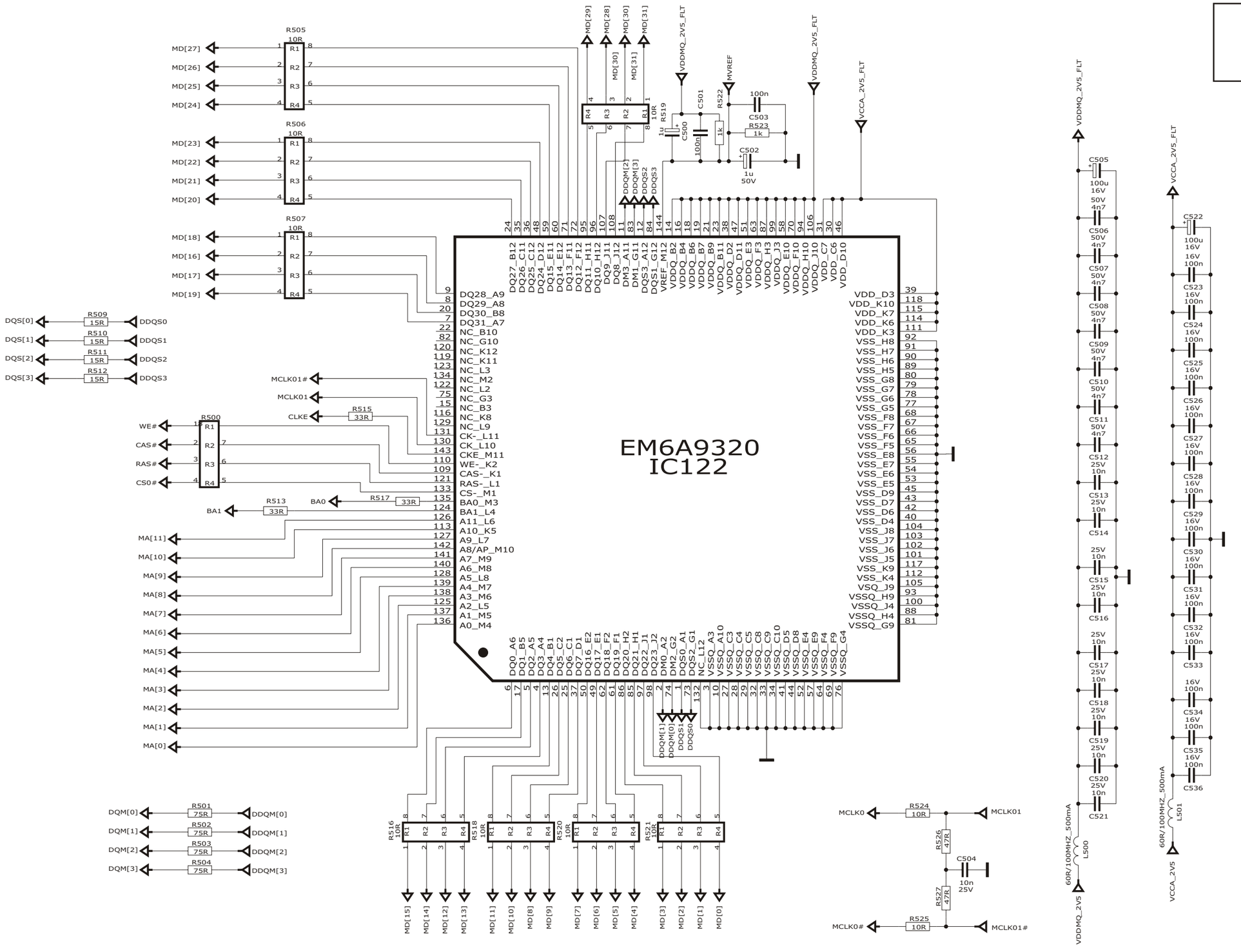
I2S OUT

HDMI INPUT

HDMI SUPPLY & GND

17MB26	MAIN BOARD CIRCUIT - SHEET 4	HITACHI

DDR RAM



17MB26	MAIN BOARD CIRCUIT - SHEET 5	HITACHI

TFT TV MCU INTERFACE

IC602
IS61LV10248

IC601
MT28F800B3W

HDMI DETECTION

DMP_IR INPUT

PANEL CONTROL

IC603
M16C/62P

UART CONNECTION FOR IDTV MODULE

UART CONNECTION FOR SW UPDATE

INT SVP

RESET MICRO-CONTROLLER

EXTERNAL SERVICE SOCKET

INTERNAL SERVICE & KEYBOARD SOCKETS

BRIGHTNESS CONTROL DIMMING

LED DRIVER CIRCUIT & IR INPUT

E2

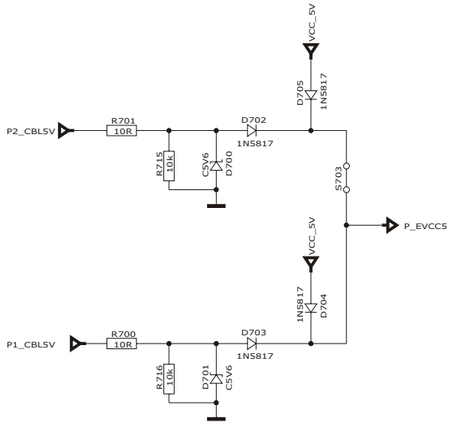
IC604
24LC32A

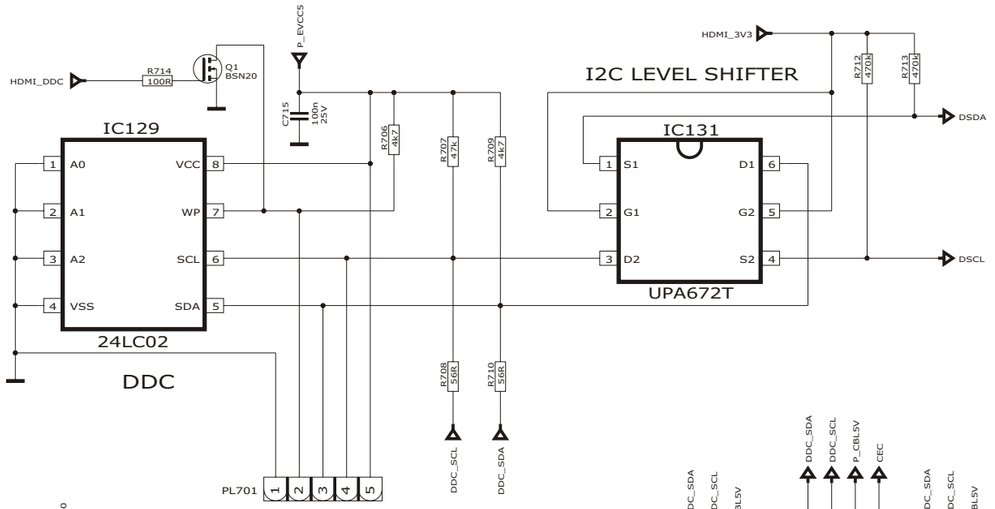
LEVEL SHIFTER

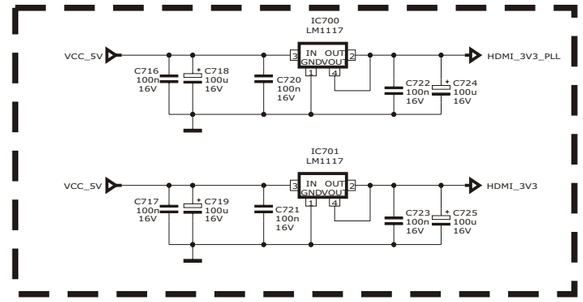
TV-LINK

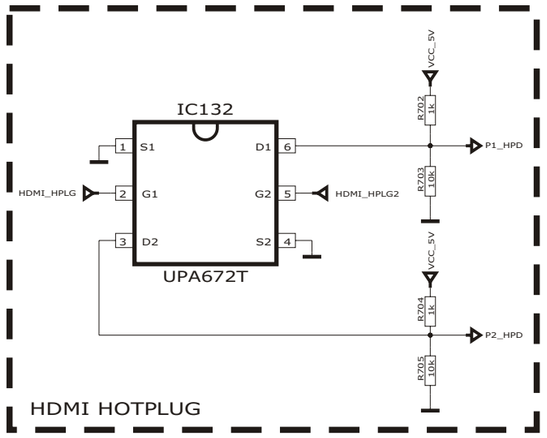
RESET SVP-LX66

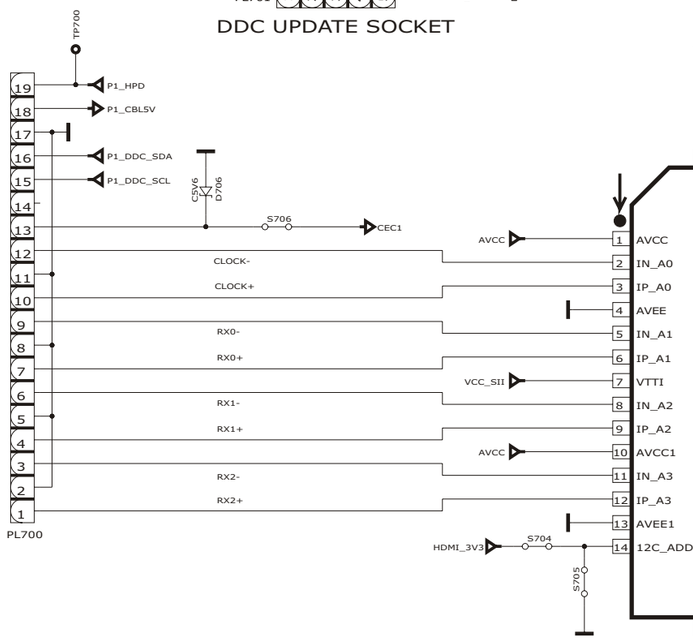
17MB26	MAIN BOARD CIRCUIT - SHEET 6	HITACHI

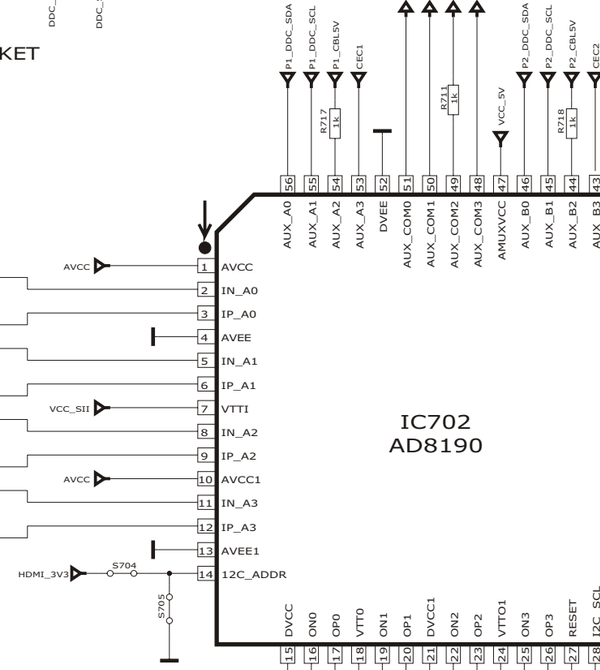


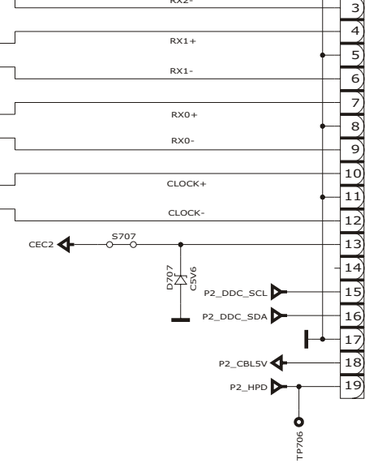


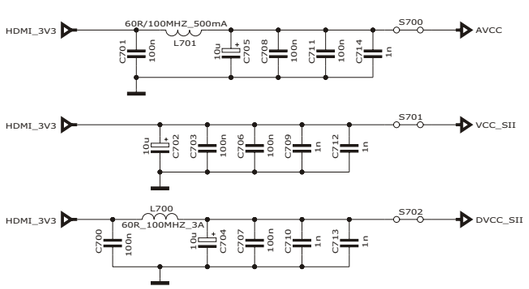


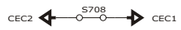








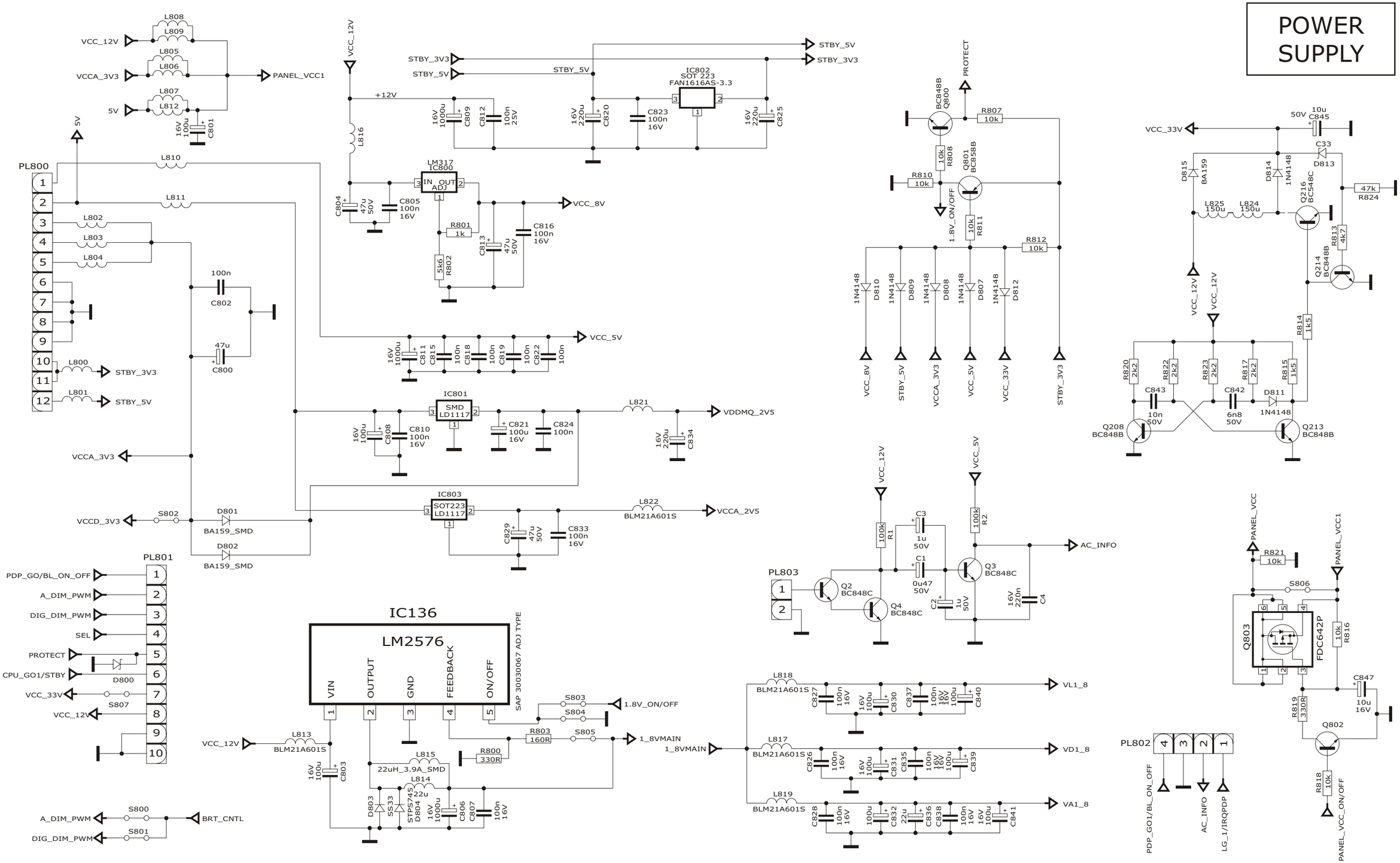




HDMI SW PART

17MB26	MAIN BOARD CIRCUIT - SHEET 7	HITACHI

POWER SUPPLY



17MB26	MAIN BOARD CIRCUIT - SHEET 8	HITACHI

UPD6111
IC101

MPEG DECODER

PROGRAMMING CONNECTOR

VCXO CIRCUIT

PI6CX100-27WE

DIGITAL AV CONNECTOR

S/PDIF

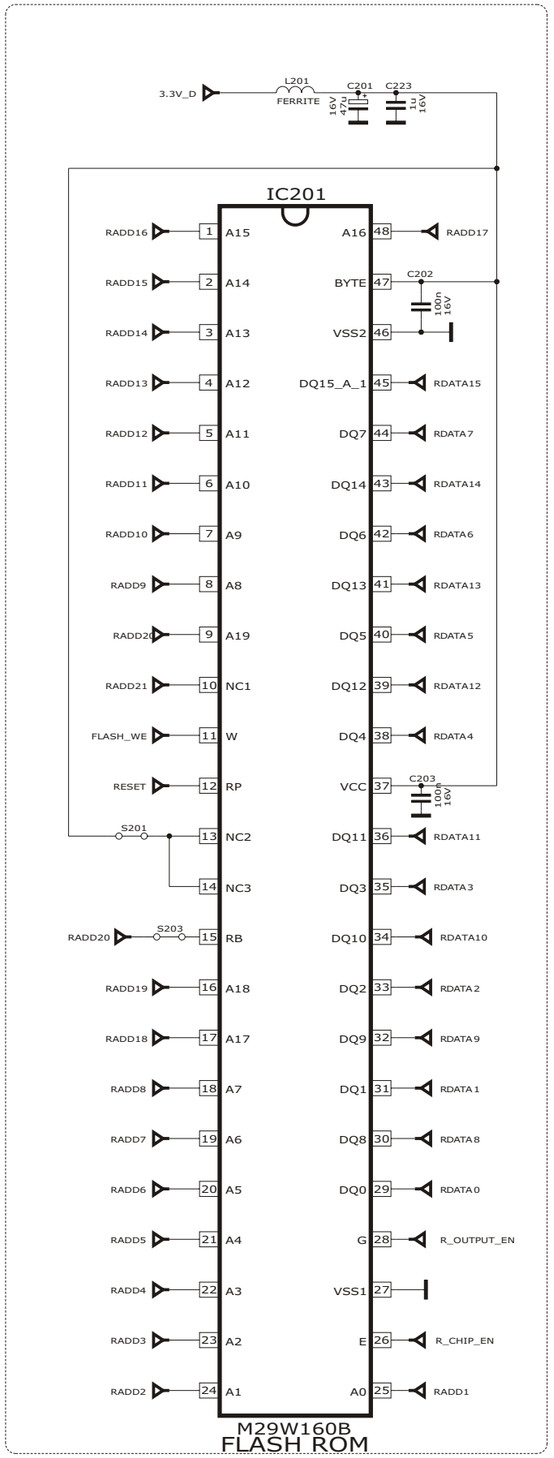
STRAP PIN JUMPERS

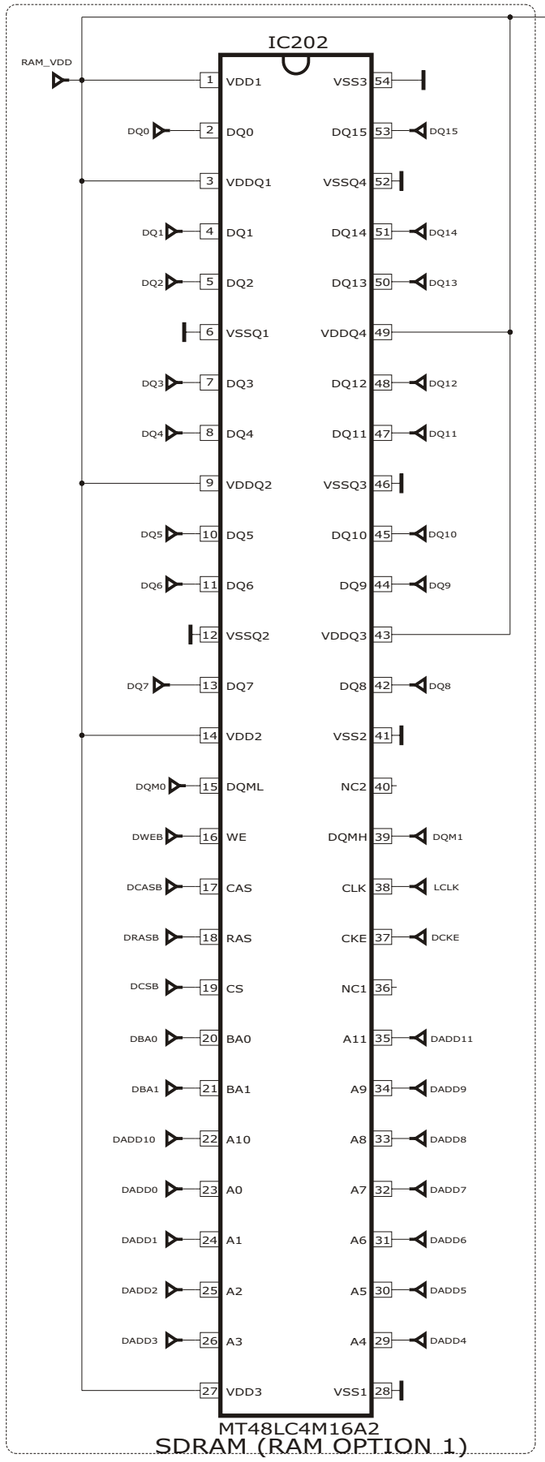
RESET CIRCUITS

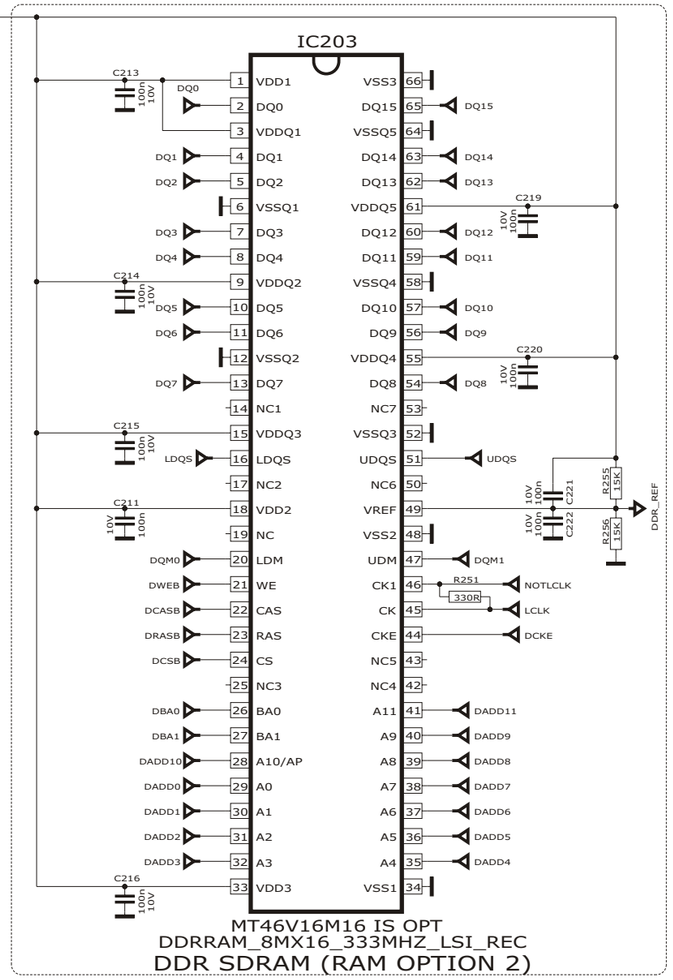
JTAG & ETAG CONNECTOR

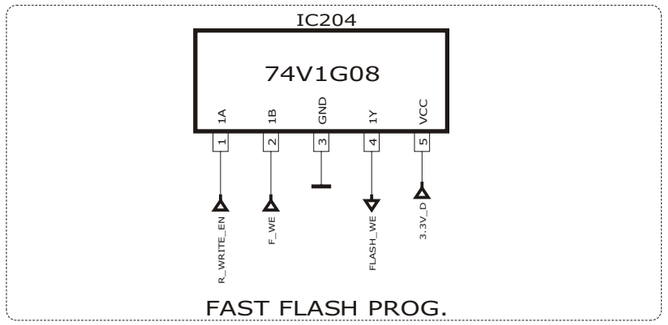
JTAG

16MB1300	IDTV MODULE BOARD CIRCUIT - SHEET 1	HITACHI

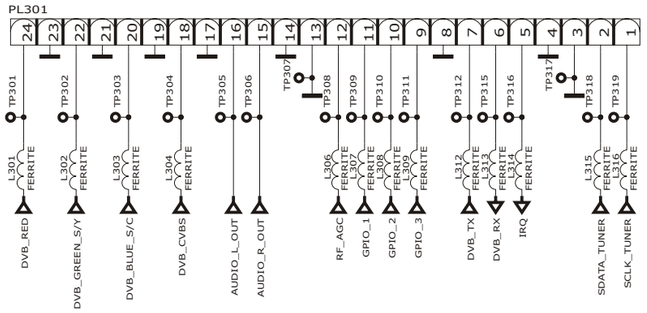




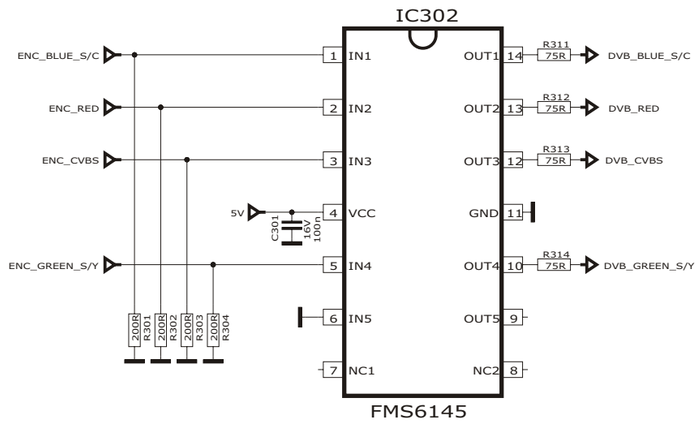




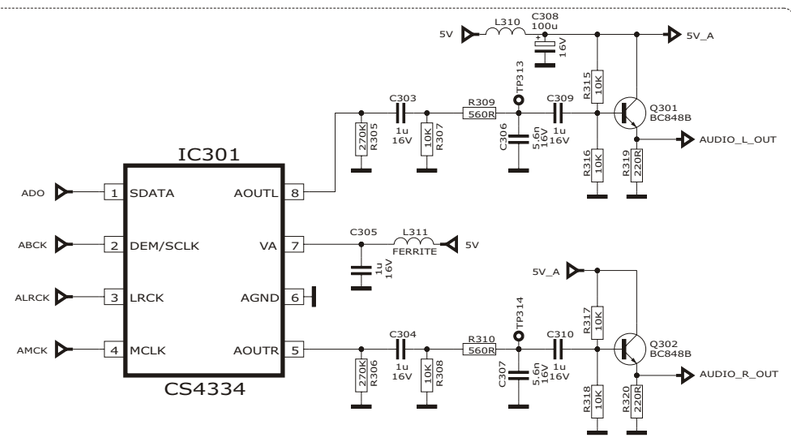
16MB1300	IDTV MODULE BOARD CIRCUIT - SHEET 2	HITACHI



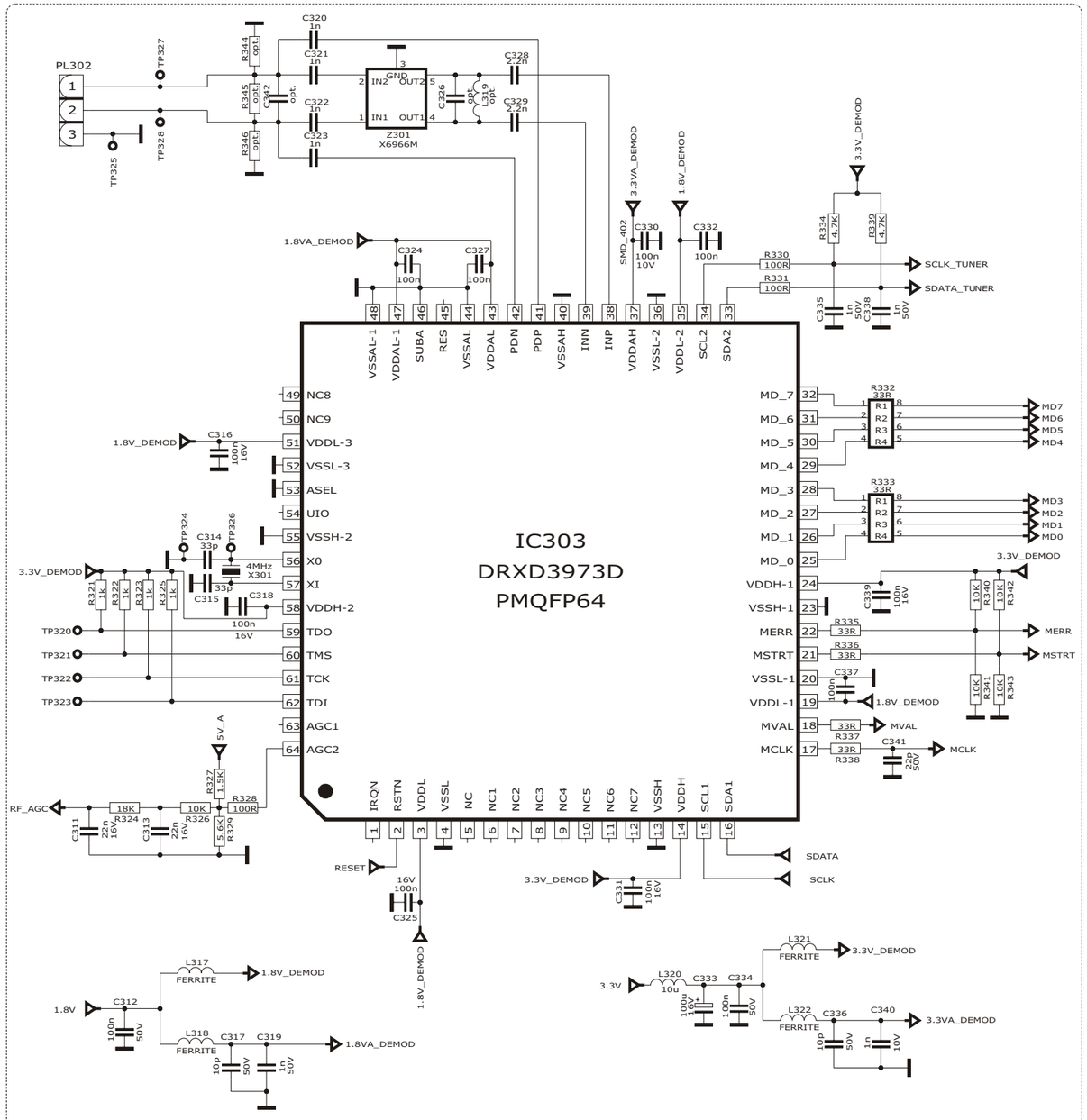
ANALOG AV CONNECTOR



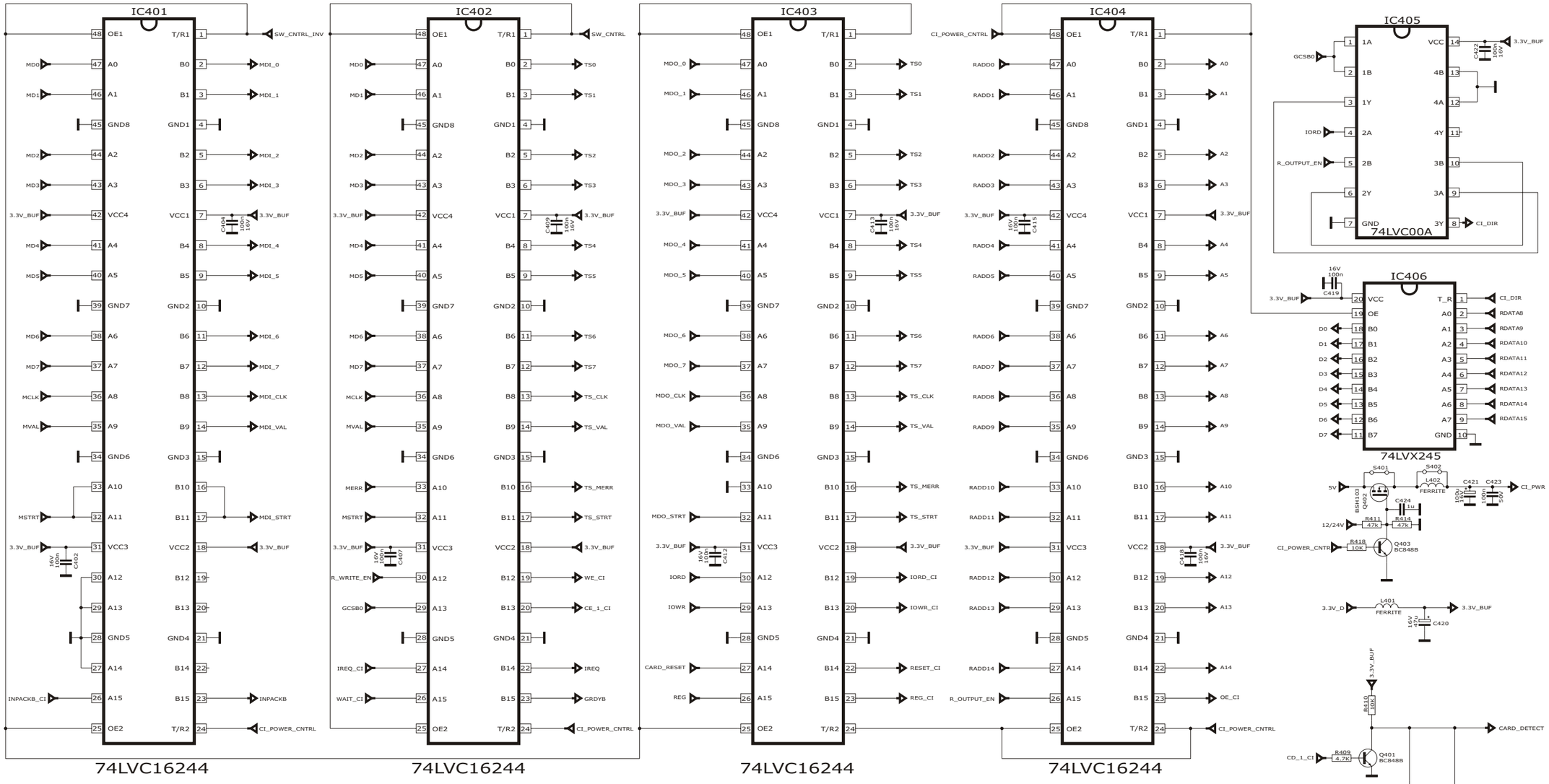
VIDEO AMPLIFIER



AUDIO DAC

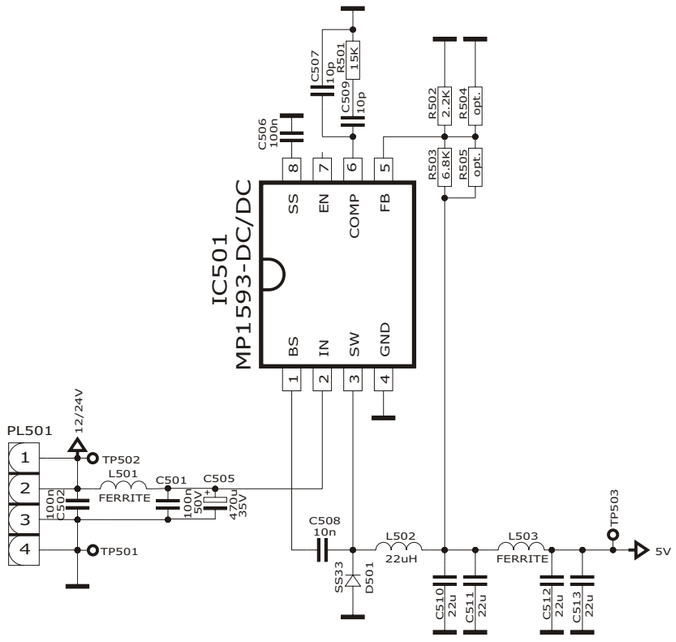


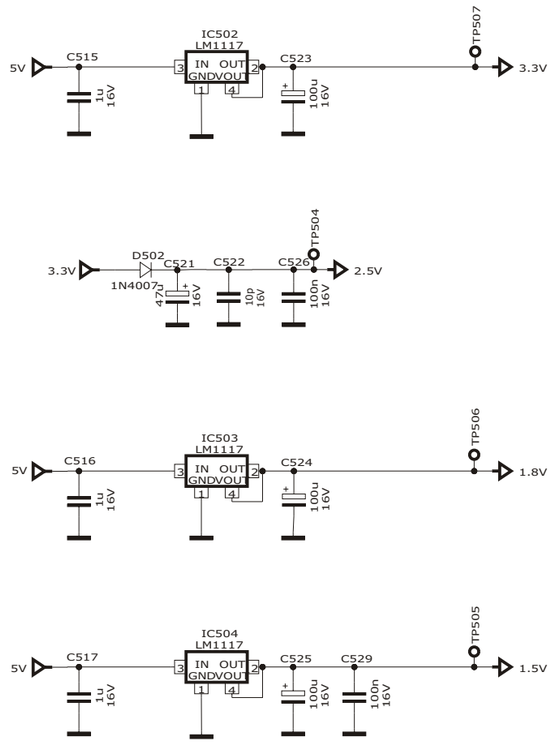
COFDM DEMODULATOR



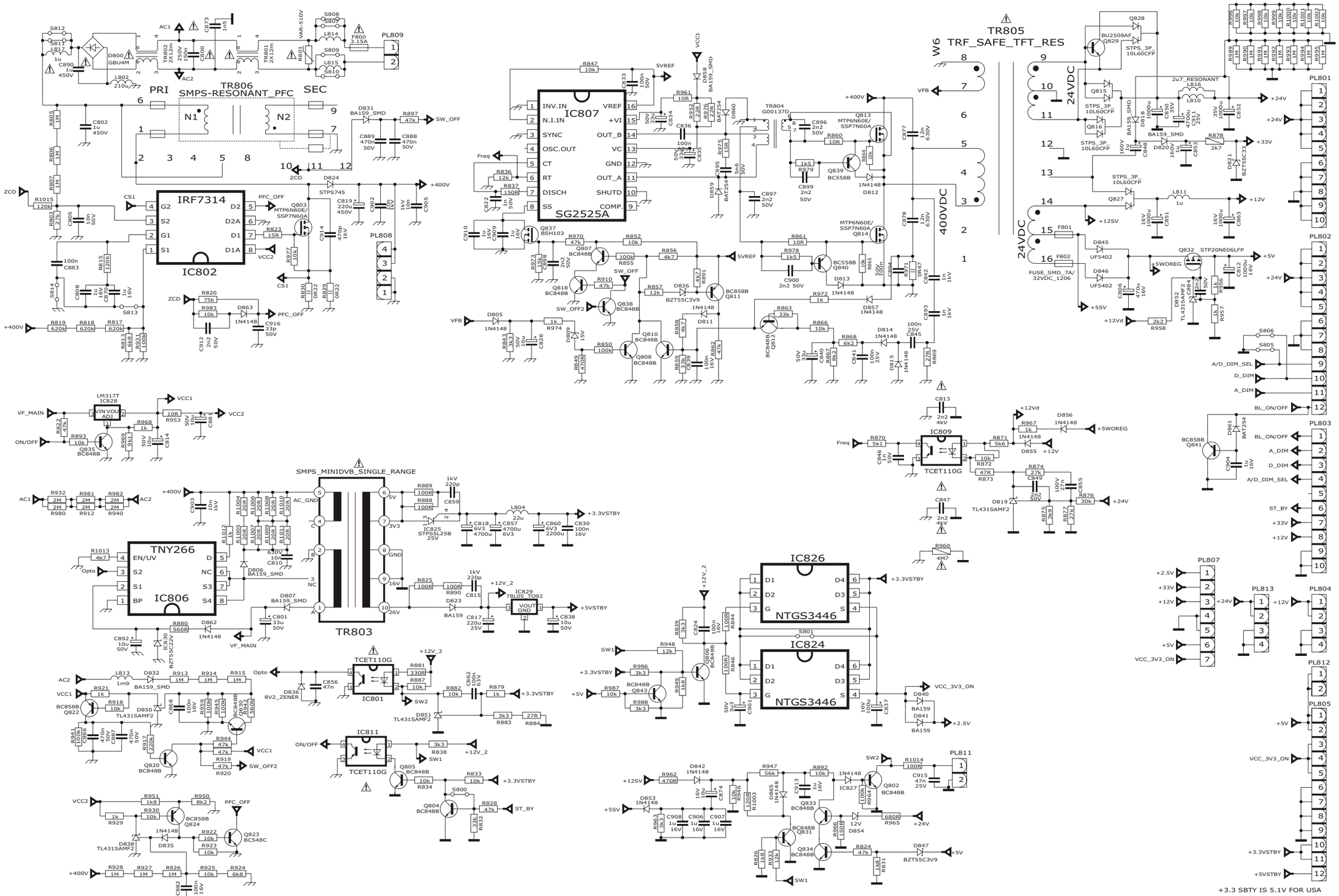
PCMCIA
INTERFACE

16MB1300	IDTV MODULE BOARD CIRCUIT - SHEET 4	HITACHI

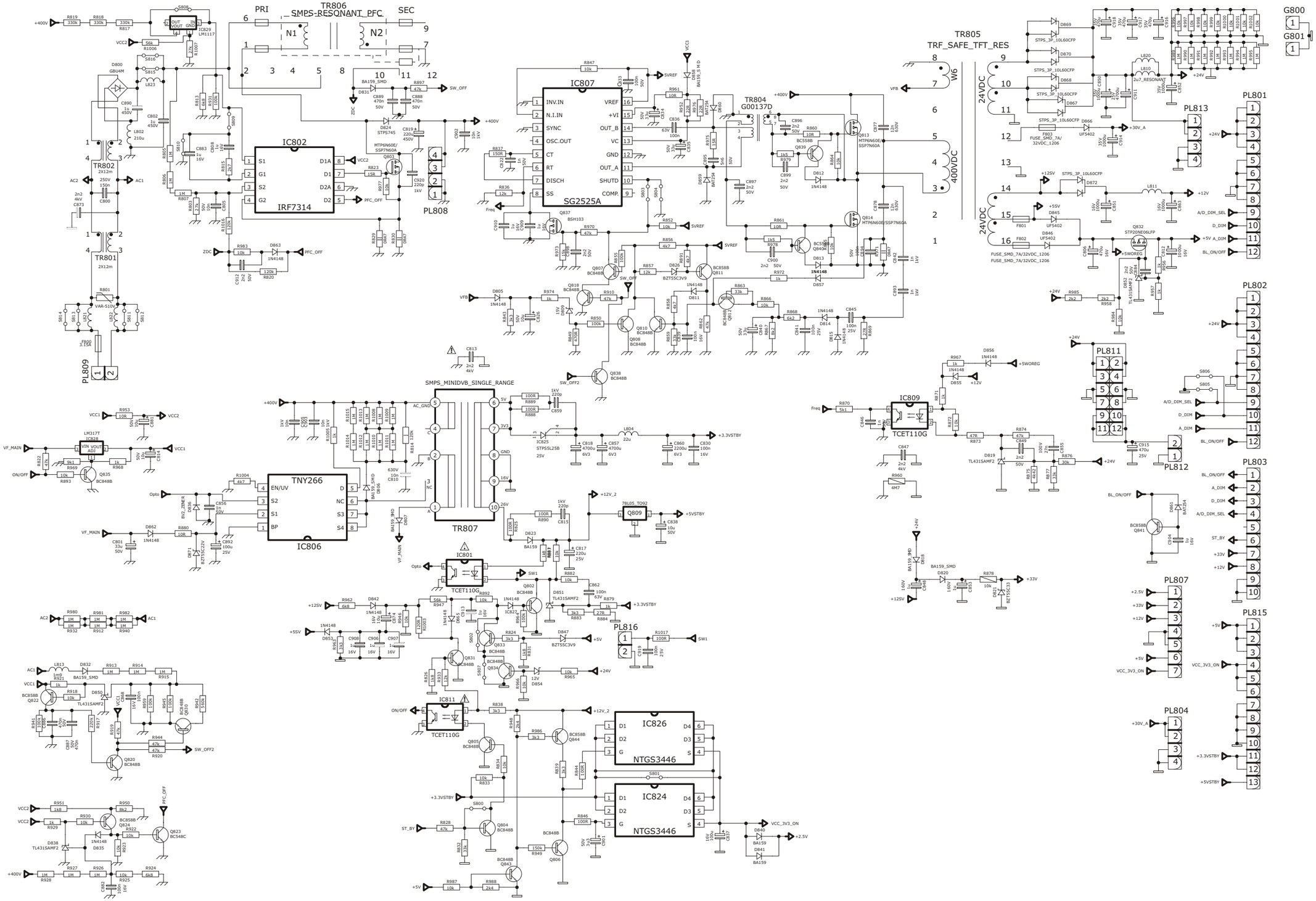




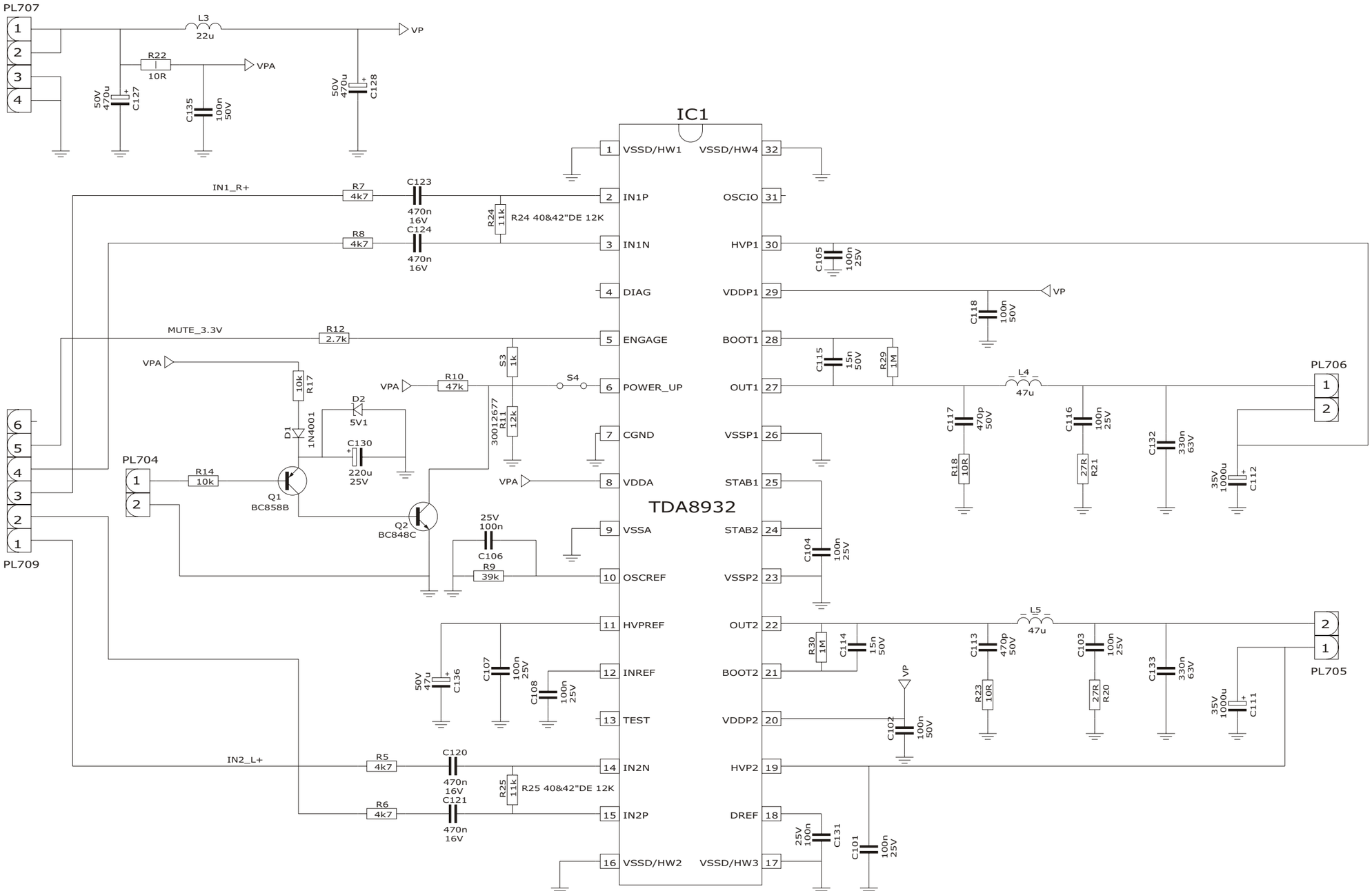
POWER
SUPPLY



17PW20	RESONANT MODE TFT POWER SUPPLY BOARD	HITACHI

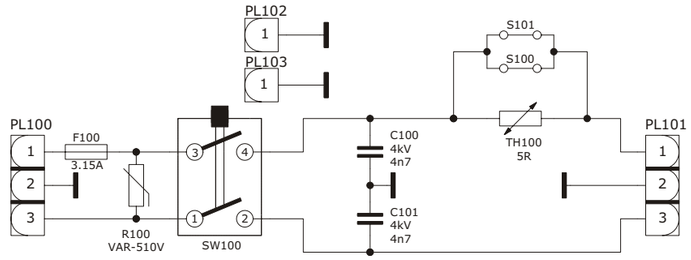


17PW16	RESONANT MODE TFT POWER SUPPLY BOARD	HITACHI

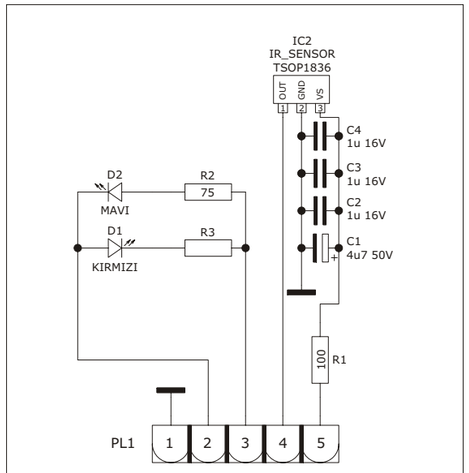


18AMP06	AMPLIFIER BOARD (CLASS-D AMPLIFIER)	HITACHI

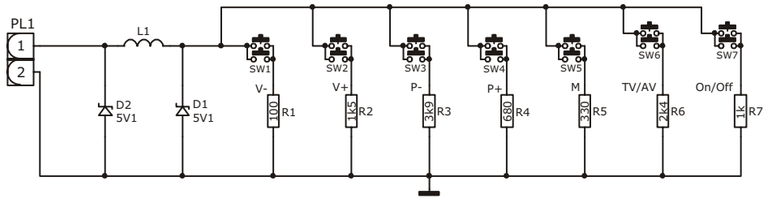
NOISE FILTER BOARD (17FL11-5)



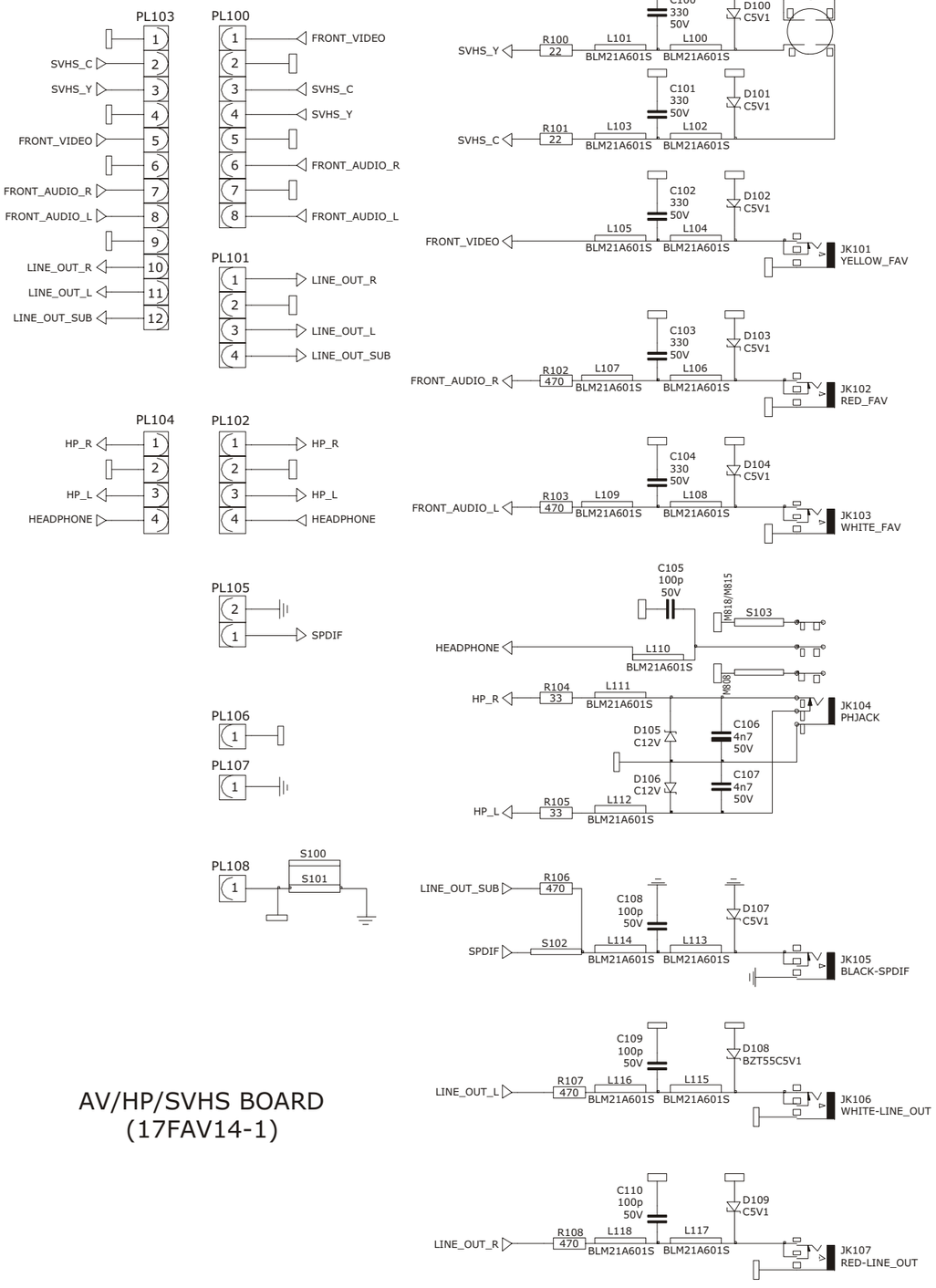
LED BOARD (17LD37-2)



KEY BOARD (17TK86)



AV/HP/SVHS BOARD (17FAV14-1)



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